Simulation Of High Gain OTA For VLSI Applications

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Abstract:-

In this paper, we deal with a high gain Proposed OTA using gain boosted current mirror and self cascode technique. Now-a-days manufacture and developer are searching ways, how to build high performance devices with smaller in size, low operating power and lighter weight. So keeping this concept in our mind we use two low power technique namely self cascode and gain boosted current mirror technique in this paper. In this we can reduce power at low voltage supply. Low static power consumption, full rail dynamic range, in case of scaling creates the perfect combination for the high performance integrated circuit .Today's electronic industry having low power is one of the key research area .Several low power electronic devices having low voltage design techniques . A low-voltage, micro-power, low-noise, high-gain, high-output swing current mirror-based operational transconductance amplifier (OTA) is presented. For this aim in mind we designed a Folded Cascode using low power techniques. We also compare power and gain characteristics of different types OTA circuit. In this paper we use self cascode technique.

1. INTRODUCTION:-

The OTA is popular for implementing voltage controlled oscillator(VCO) and filter(VCF) for analog music synthesizers ,because it can act as a two-quadrant multiplier as we will see later. Viewed from a slightly different angle an OTA can be used to implement electrically tunable resistor that is referenced to ground , with extra circuitry floating resistors are possible as well. Operational transconductance amplifiers (OTAs)[1] are the main building blocks of many circuits where the OTA tends to dominate the power consumption. The key performance parameters of OTAs are output swing, DC gain, and gain bandwidth (GBW). The output swing is of great importance in low-voltage (LV) and low-power (LP) [2-5]designs. Single-stage OTAs tend to be more power efficient than two-stage OTAs, because no power is wasted in driving the compensation capacitance in single-stage OTAs. The typical voltage gain of the CMOTA is about 20–40 dB in submicron technologies. With many applications, the required DC of OTAs is

much higher than 40 dB. There are sevral type of technique but we will use some important technique in this paper. In case of CMOTA ,the CMOTA having gain boosting current mirroring technique which this technique can enhance the gain without additional power consumption . Here many type of techniques are included for low power and high gain OTA. In this paper we will work on self cascode technique.

1.2 SELF CASCODE TECHNIQUE:-

Basically the use of self cascode technique in this paper to reduce power and increase the gain of OTA. The CMOTA having gain boosting current mirroring technique which this technique can enhance the gain without additional power consumption. The self-cascoding is another technique that can increase the DC gain of CMOTAs.[6] . A self-cascode is a 2-transistor structure as shown in figure, which can be treated as a single composite transistor. The effective gm for the composite transistor is as given below, where M2 have to be in saturation and M1 in liner region.

$$g_m(effective) = (g_{m2}/m) = g_{m1} \quad (1)$$

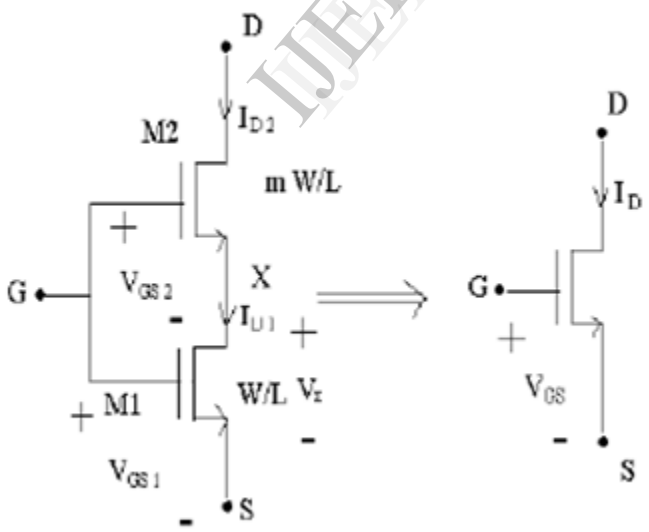


Figure 1 : Self Cascode NMOS transistor with its equivalent circuit

In case of ohmic region,drain current is given as:-

$$I_{D1} = \beta 1 \left(V_{in} - V_{TN} - \frac{vx}{2}\right) v_x \quad (2)$$

In case of saturation region , drain current is given as:-

$$I_{D2} = \left(\frac{\beta 2}{2}\right)(V_{in} - V_x - V_{TN})^2 \quad (3)$$

From (1),(2) by splitting we get:-

$$I_D = \left[\frac{\beta_2\beta_1}{2(\beta_2+\beta_1)}\right][V_{in} - V_{TN}]^2 \quad (4)$$

In equation (3) , $\frac{\beta_2\beta_1}{(\beta_2+\beta_1)}$ is the effective gain so its value is equal to:-

$$\beta_{effective} = (\beta_2\beta_1)/(\beta_1 + \beta_2) \quad (5)$$

$$\beta_2 = m\beta_1 \quad (6)$$

$$\beta_{effective} = [m/(m+1)]m1 = [1/(m+1)]\beta_2 \quad (7)$$

if m>>1 so we get:-

Effective gain is nearly equal to β_1

$$\beta_{effective} \approx \beta_1 \quad (8)$$

Where $\beta = \mu c_{ox}(w/l\ )$are called the transconductance parameter

2. Circuit design:-

The single-stage OTA that can provide rail-to-rail output swing is the current mirror-based OTA (CMOTA) which is shown in Figure 2. The typical voltage gain of the CMOTA is about 20–40 dB in submicron technologies. With many applications, the required DC of OTAs is much higher than 40 dB.

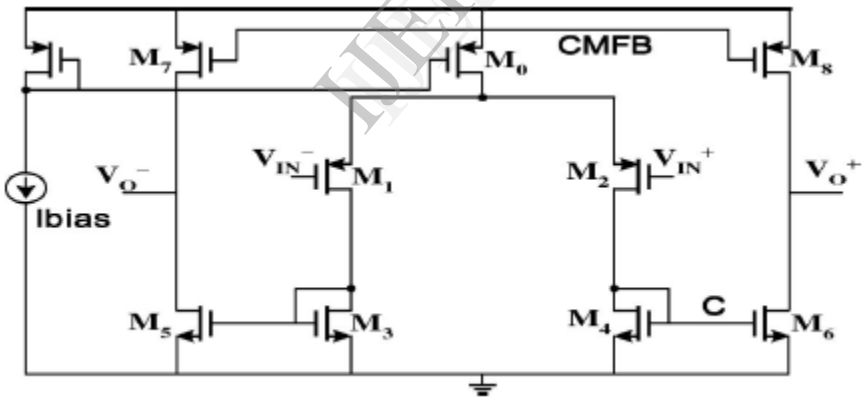


Figure 2. The conventional current mirror OTA

In case of figure 2 ,there are many technique to increase the gain of the CMOTA. By using gain boosting technique in CMOTA. Which can enhance the gain by 10–20 dB without additional power consumption In figure 3 a portion of input transistor (M1/M2) which can be splitted from current mirror transistor (M3/M4) In the sense of the Dc gain of the OTA is boosted by 1/(1-k) times .If K factor close to 1 the OTA gain can be increased significantly .So higher the K factor ,the higher the impedance [7-9].

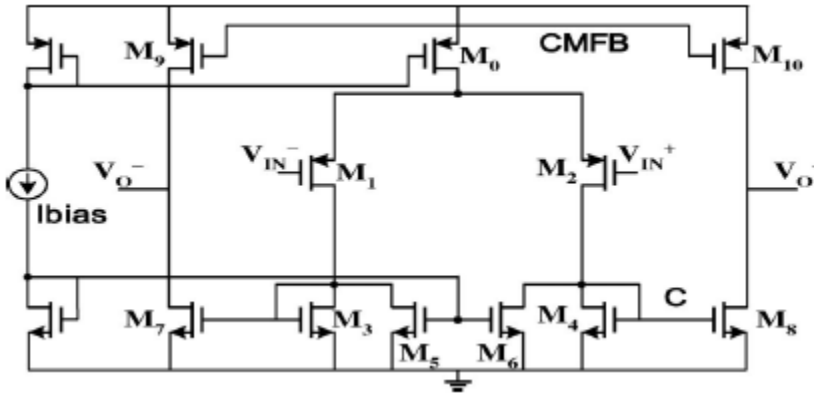


Figure3. The current mirror OTA with gain enhancement

Therefore, the increase in k factor is limited, and the actual gain enhancement is not higher than 20 dB. The self-cascoding is another technique[10-11] that can increase the DC gain of CMOTAs while still providing enough output voltage swing as shown in Figure 4. In Figure 4, for high output voltage swing, M5/M6/M11/M12 and M7/M8/ M9/M10 are biased to operate in strong and weak inversion regions, respectively. Using the OTA topology shown in Figure 4, a DC gain of 66 dB with an output voltage swing of 620 mV out of 1.2 V supply.

3. The proposed OTA:-

The proposed OTA combines the two previous techniques, gain boosted current mirroring and self cascoding. the two techniques allows a very high DC gain in proposed OTA. The proposed OTA is designed based on a 0.18 mm CMOS with 1.0 V supply. In Figure 5

$$Vg8 = Vgs8 = Vth + Vdsat8 \quad (9)$$

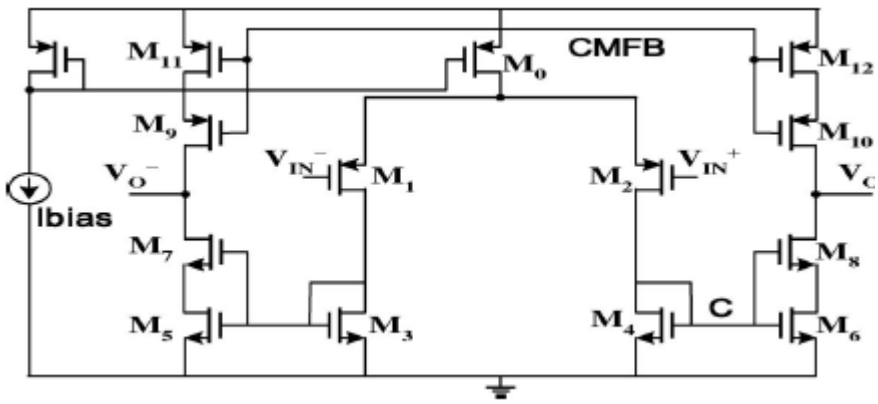


Figure 4 The current mirror OTA with self-cascoding output stage

where Vg8, Vgs8, Vth, and Vdsat8 are gate, gate-source, threshold, and saturation voltages of M8. The drain voltage of M8 should be larger than the saturation voltage Vdsat8.

Vd8 = Vgs8 -Vgs10 =Vth + Vdsat8 -Vgs10 > Vdsat8 (10)

if Vth 4 Vgs10, i.e. the transistor M10 has to be biased in weak inversion region. In order to force M4/M8 to operate under strong inversion, their channel lengths are chosen relatively long. The proposed OTA is designed to work with micro-power; therefore, it is easy to bias M10 to operate under a weak inversion region by increasing its size .

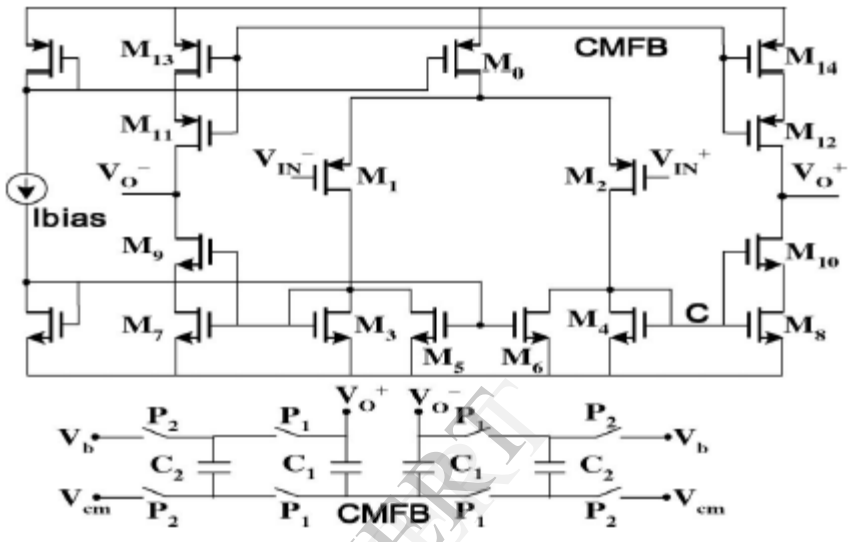


Figure 5 The proposed gain boosted self-cascoding current mirror OTA

4.Results and Discussion: Figure 6 and 7 shows the frequency response and the step response of the proposed OTA. The proposed OTA shows a DC gain of 90 dB with GWB product of 700 kHz for a load capacitor value of 1 pF while achieving the phase margin of 50. The phase margin lies between the gain and phase. In case of figure 7 shows time response of proposed OTA its shows the relation between input as well as output voltage . By increase the value of m ,we can further increase the gain of the proposed OTA with the low power consumption but the condition of self cascode should be maintained.

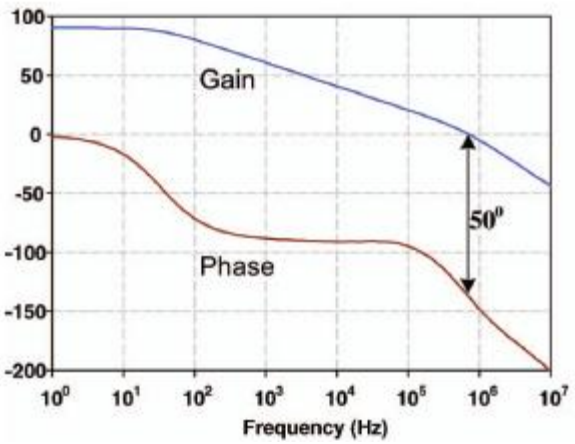
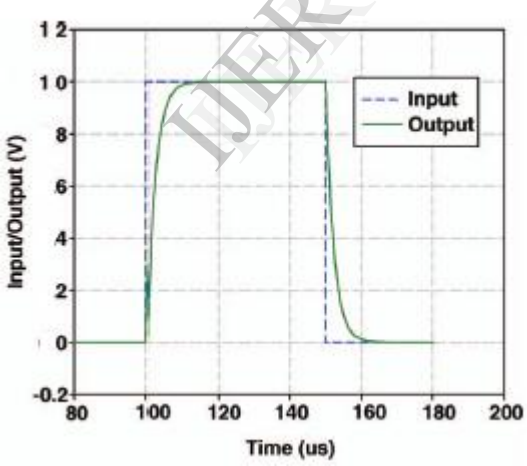


Figure 6. Frequency response of the proposed OTA

This proposed circuit have been employed in a variety of situation from increasing the gain in amplifier medium available bandwidth. The channel length and width of the two transistor can be optimized for the largest increase in the output resistance. The input referred noise of the OTA at 10 kHz is 78 nVrms/ sqrt (Hz), and output voltage swing is 600 mV while dissipating 750 nW from 1.0 V supply.



. Figure 7. Time response of the proposed OTA

In figure dotted line shows input voltage and dark line shows output voltage. The output voltage line show slightly fluctuate over the input voltage. It provide high output impedance to give high output gain so it is useful for low voltage design.

4.1 Power Consumption:

In case of previous result, proposed ota having power consumption 1.038805e-002watts .

Now In Proposed Folded Cascode OTA using Self Cascode Technique and the amount of average power consumption is 4.44231e-002 Watts. So the power consumption in proposed folded cascade OTA is higher than previous result. So self cascode technique is more suitable to reduce power consumption.

5.CONCLUSION:

In this paper from simulation result ,figures we conclude that the gain of the structure increases which the regular cascade structure are avoided, but decrease the output signal swing. It is capable in low voltage design which it provide high output impedance to give high output gain. In case of low power consumption ,we increase the gain of the proposed gain boosted OTA The proposed OTA, implemented in 0.18 mm CMOS, shows a DC gain of 90 dB, GWB product of 700 kHz, phase margin 50 ,an output voltage swing of 600 mV while dissipating 750 nW from 1.0 V supply. The gain boosted current mirroring and self-cascoding techniques are used effectively for calculating A low-voltage, micro-power, low-noise, high-gain, high-output swing OTA. In Future there are many possibilities of research on this topic.

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