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Study of Conventional Versus Energy Recovery Low Power Clocking Schemes in CMOS Digital VLSI

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***Abstract*—In today's high-performance VLSI circuits, power dissipation is one of the major design challenges faced by the designers. Clock network accounts for a significant fraction of the total power dissipation in a VLSI chip. Low power clock solutions indirectly helps in bringing down the total power dissipation of the chip. This paper puts an insight into the various conventional low power clocking schemes, its limitations and the energy recovery low power clocking schemes, which is the emerging trend in VLSI industry.**

Keywords—clock power reduction; adiabatic swtching; energy recovery; half swing clocking; resonant clocking;clock gating

I. INTRODUCTION

With the continuing evolution of integrated circuits, and the increasing demands for more functionality, circuit complexity is constantly increasing. Power reduction has become a major challenge faced by today's VLSI designers. This is setting the limit on the amount of functionality that can be integrated and on the achievable performance. A major contributor to the total power dissipation in modern high performance microprocessors is the clock distribution network. Conventional low power clocking schemes are based on a power hungry clock distribution network, which has its own limitations. Various conventional low power clocking schemes, along with energy recovery techniques for clock power reduction are discussed in this paper. Clock power reduction brings down the total power dissipation of the chip, thereby enabling further increase in functionality.

II. IMPORTANCE OF POWER REDUCTION

One of the most important parts of a synchronous VLSI chip is the clock network, since it has a significant influence in the speed, area and power dissipation of the overall system. Clock networks dissipates about 20-50% of total power on a chip. With the growth in low power, high performance portable applications, it has become necessary to develop strategies to significantly reduce power dissipation of the clock network since this will lead to a major reduction in the overall power dissipation of the chip. Carrying large loads and switching athigh frequency, dynamic power dissipation is the most dominant component of clock power dissipation in VLSI. [1]The dynamic power dissipated by switching the clock is given by the expression:

$$P_{clk} = C_L f_{clk} V_{dd} V_{sw}$$

Where P_{clk} - power dissipated in clock network, C_L – total load driven by clock, V_{dd} - supply voltage, f_{clk} – clock frequency, V_{sw} - clock swing

When $V_{sw} = V_{dd}$, the above equation reduces to

$$\boldsymbol{P_{clk}=C_L f_{clk} V_{dd}^2} \quad \textbf{(1)}$$

III. CONVENTIONAL POWER REDUCTION TECHNIQUES

Conventional clock transmission method is shown below:

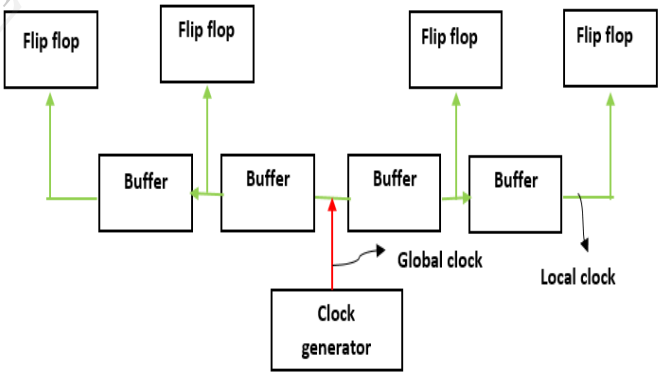

Fig. 1. Conventional clock transmission

Majority of the clock power is dissipated in the intermediate buffers. Conventional clock power reduction techniques are discussed below [2].

A. *Frequency Reduction*

Since there is a linear relationship between frequency and clock power dissipation (1), frequency reduction helps in reducing clock power. Reduction in frequency reduces the amount of operations that can be performed and hence the performance. This can be compensated by going for parallelism and pipelining techniques, with an area penalty. These additional hardware further escalates the clock load, thereby nullifying the power reduction. Hence,

best choice is to go for a frequency reduction in blocks where the concern is throughput and not performance.

B. *Supply voltage reduction*

Clock power is directly proportional to the square of supply voltage (1). Considerable amount of clock power saving is possible by supply voltage reduction [7]. As the supply voltage is scaled down, delay increases and performance degrades. Hence, voltage reduction should be done on those blocks whose required computation speed is less.

Dynamic supply voltage and frequency scaling during operation is a commonly used technique to reduce clock power. When the required computation speed is low, both supply voltage and clock frequency of thechip is reduced, leading to considerable clock power and total power reductions.

C. *Clock load reduction*

Clock load reduction helps in reducing total clock power, as per (1). One way of reducing clock load is by downsizing transistors in the flipflops. This comes with a performance penalty since downsizing the transistor lowers its current drive.

D. *Clock gating*

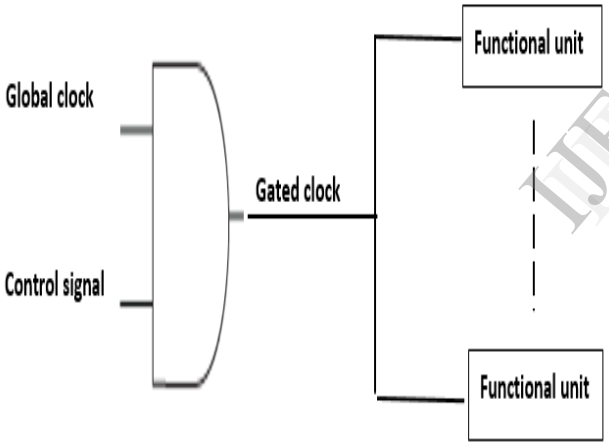

Fig. 2. Clock gating technique

It is the most popular conventional clock power reduction technique. When the clock signal of a functional module is not required for a period of time, a gating function is used to turn off the clock feeding the module.[3] In the figure, an AND gate is used to accomplish this. Clock is masked using a 'control' signal,which blocks the clock signal coming from the clock source, to functional units further in the network. The 'control' signal should be enabled and disabled at a much slower rate compared to the clock frequency or else power required to drive the 'control' signal may outweigh the power saving.

E. *Half swing clocking*

In this technique, all the clock swings are reduced to half the supply voltage. Rest of the logic circuits will work with full supply voltage. This ensures maximum power reduction with minimal speed degradation.[3],[4]

Two separate clock signals are used for NMOS and PMOS transistors. Clock for NMOS transistor swings from 0 to $V_{dd}/2$ and the clock for PMOS transistor swings from V_{dd} to $V_{dd}/2$.The technique helps in reducing clock power by 25%.

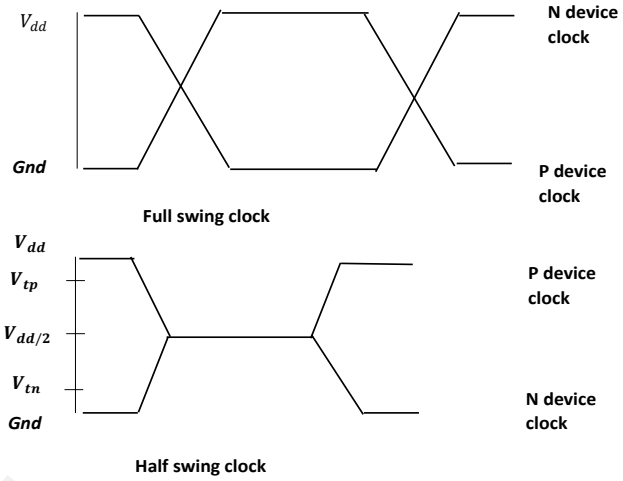

Fig. 3. Reduced clock swing technique

IV. ENERGY RECOVERY TECHNIQUES

Energy recovery techniques [2],[5] achieve low power dissipation by restricting current to flow through devices with low voltage drop and by recycling the energy stored on their capacitors. A sinusoidal clock signal is made use of in this technique rather than the conventional square wave clock.This technique can be applied to the clock network since the clock signal is typically the most capacitive signal .Majority of clock power saving is achieved by eliminating buffers from the clock network. Various energy recovery techniques adopted at industry level are discussed below.

A. *Adiabatic switching*

The term 'adiabatic' means that all charge transfer occurs without generating heat. Total energy dissipation during a conventional switching event is $C_L V_{dd}{}^2$, all of which is dissipated as heat.

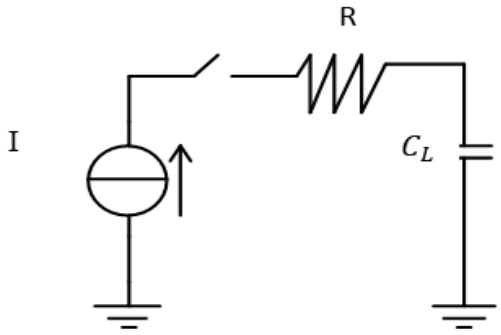

Fig. 4. Adiabatic switching technique

The concept of adiabatic switching [6] can be described using a constant current source I driving the clock load capacitance C_L through a resistive path R, which is the channel resistance in a mosfet. The energy dissipated in R during the charging event is given by the expression:

$E_{D,resistor} = V_{resistor} \cdot Q_{capacitor}$

$$= \frac{RC_L{}^2 V_{dd}{}^2}{T} \quad (2)$$

Where V_{dd} – supply voltage, T – time taken to charge C_L between 0 and V_{dd} .

Thus it is possible to reduce energy and hence power by increasing the switching time. Slow transition times makes this technique less suitable for multi-GHz clocked systems.

B. Bufferless LC tank resonant clocking

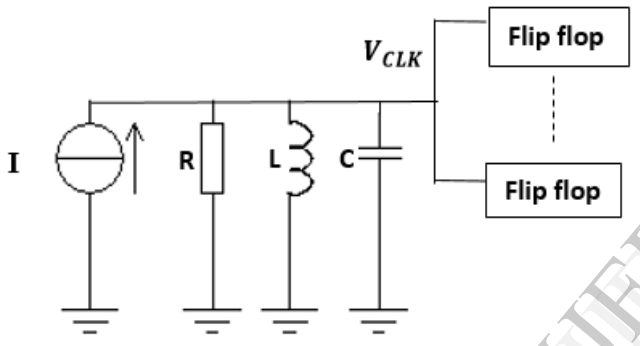

Fig. 5. LC resonant clocking technique

The technique makes use of an LC oscillator [2] in parallel resonance to drive the entire clock load without using any intermediate buffers. Elimination of intermediate buffers helps to save power to a great extend. At resonance, impedance of the parallel LC combination will be very high. Hence power will be dissipated only in R, which is the sum of parasitic resistance in both inductor and capacitor.

$$\frac{P_{resonator\ clock}}{P_{conventional\ clock}} = \frac{3\Pi}{4Q} \Big/ \sum_{n=0}^{n=N-1} \frac{1}{\lambda^n} \quad \textbf{[2] (3)}$$

Where Q- quality factor of the resonant circuit, N- no of buffer stages and λ- tapering factor of conventional clock buffers.

For λ =3 , the expression reduces to

$$\frac{P_{resonator\ \ clock}}{P_{conventional\ \ clock}} = \frac{\Pi}{2Q}$$

This implies that for a Q> Π , the resonant clocking saves more than 50 % power than conventional clocking scheme.

C. Synchronised oscillator driven clocking

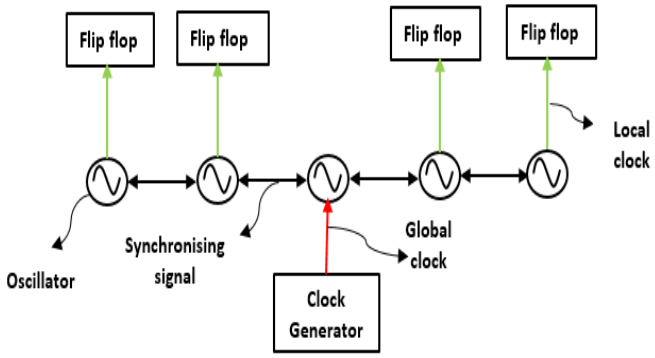

Fig. 6. Synchronised oscillator clocking technique

In this technique, an oscillator is built into each functional unit [8] .All the oscillator outputs (local clocks) are then synchronised with the global clock. As a result, the frequency and phase of the local clocks match the frequency and phase of the global clock. The signal between each oscillator required for synchronization require less amplification compared to the amplification at intermediate buffers in conventional clocking schemes. This technique has resulted in a 75% reduction in the clock power consumed by a 16 GHz clock distribution circuit, resulting in a 20% reduction in the overall power consumed.

D. Energy recovery clocked flipflops

Flip-flop is a major part of synchronous circuits in digital CMOS VLSI. The type and structure of the flip flop used determine the amount of clock load and hence has a large impact on the overall system power consumption. The energy recovery clocked flip-flops enable energy recovery from the clock network, resulting in significant energy saving. Various circuits are implemented at industry level using various type and structure of flip flops.

Multi-Bit Flip-Flop is one approach [9], in which some flip flops are replaced by smaller amount of multi bit flip flops. When flip flops are reduced in number, number of clock sinks in clock tree reduces and hence the power consumption. Various other techniques are proposed in papers [10],[5].

V. CONCLUSION

The power consumption of the clock tree dominates over 40% of the total power in high performance VLSI designs. Hence, low power clocking schemes are promising approaches for low power design. Conventional clock power reduction techniques along with their limitations are discussed. Various energy recovery techniques adopted at the industrial level are also reviewed in this paper.

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