

# Study of Performance Analysis of H-Bridge VSI with Sinusoidal Pulse Width Modulation

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**Abstract**—The Voltage Source Inverter is generating AC square wave and sinusoidal current. The best performance of VSC can be achieved by different modulation techniques. With SPWMVSC generate sinusoidal voltage or current which is useful for household applications also.

Using controlled inverter speed control of machines becomes finer. For testing of quality of inverter output voltage or current, %THD and switching frequency are two important parameters. Pulse Width Modulation (PWM) is commonly used in inverter control. PWM switching technique is widely used in power electronics to get proper sequence to on and off of the power switches to generate voltage pulses and sinusoidal current. The pulse width modulation inverter are extensively used in power electronic, because of its circuit simplicity and rugged control scheme. SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. In this paper single-phase inverters and its %THD is analyzed. Simulation results are obtained using MATLAB/Simulink environment for effectiveness of the study.

**Keywords**—SPWM; %THD; Simulink; Single-phase inverter.

## I. INTRODUCTION

The dc-ac converter, also known as the inverter, converts dc power to ac power at desired output voltage and frequency. The dc power input to the inverter is obtained from an existing power supply network or from a rotating alternator through a rectifier or a battery. AC loads require constant or adjustable voltages at their input terminals. When such loads are fed by inverters, it's essential that output voltage of the inverters is so controlled as to fulfill the requirements of AC loads. This involves coping with the variation of DC input voltage, for voltage regulation of inverters and for the constant volts/frequency control requirement. There are various techniques to vary the inverter gain. The most efficient method of controlling the gain (and output voltage) is to incorporate pulse-width modulation (PWM) control within the inverters. The carrier based PWM schemes used for inverters is one of the most straight forward methods of describing voltage source modulation realized by the comparison of a modulating signal (sine) with carrier signal (triangular). Normally machines do not perform smoothly due to large amount of %THD, which causes noise, vibration and heating in

machines. So, proper system need to be developed to minimize %THD.

## II. INVERTERS

### A. Introduction

The main objective of static power converters is to produce an AC output waveform from a DC power supply. For sinusoidal ac outputs, the magnitude, frequency, and phase should be controllable. According to the type of ac output waveform, these topologies can be considered as voltage source inverters (VSIs), where the independently controlled ac output is a voltage waveform. These structures are the most widely used because they naturally behave as voltage sources as required. Similarly, these topologies can be found as current source inverters (CSIs), where the independently controlled AC output is a current waveform.

### B. Single-phase VSI

First, Single-phase voltage source inverters (VSIs) can be found as half-bridge and full-bridge topologies. Although the power range they cover is the low one, they are widely used in power supplies, single-phase UPSs, and currently to form elaborate high-power static power topologies, such as, the multi-cell configurations.

1) *Half-bridge*: Figure 1 shows the power topology of a half-bridge VSI, where two large capacitors are required to provide a neutral point N, such that each capacitor maintains a constant voltage  $v_i/2$ . Because the current harmonics injected by the operation of the inverter are low-order harmonics, a set of large capacitors ( $C_+$  and  $C_-$ ) is required. Table 1 shows ON & OFF state of the switches & corresponding voltage  $v_o$ .

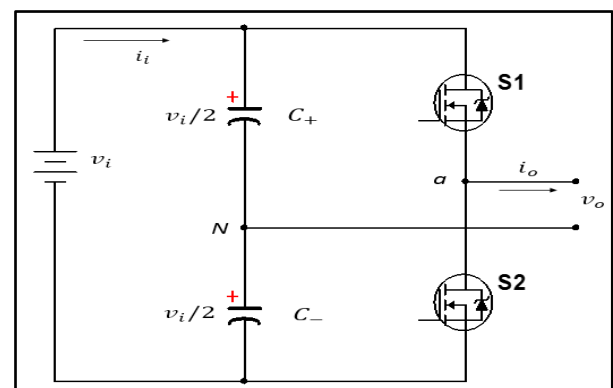


Fig. 1 Single-phase Half-Bridge VSI

TABLE 1 SWITCH STATES FOR A HALF-BRIDGE SINGLE-PHASE VSI

State	State	$v_o$
$S_1$ is on & $S_2$ is off	1	$v/2$
$S_2$ is on & $S_1$ is off	2	$-v/2$
$S_1$ is off & $S_2$ is off	3	$v/2$

2) *Full-Bridge*: Figure 2 shows the power topology of a full-bridge VSI. This inverter is similar to the half-bridge inverter; however, a second leg provides the neutral point to the load. It can be observed that the ac output voltage can take values up to the dc link value  $v_i$ , which twice that is obtained with half-bridge VSI topologies. Table 2 shows ON & OFF state of the switches & corresponding voltage  $v_o$ .

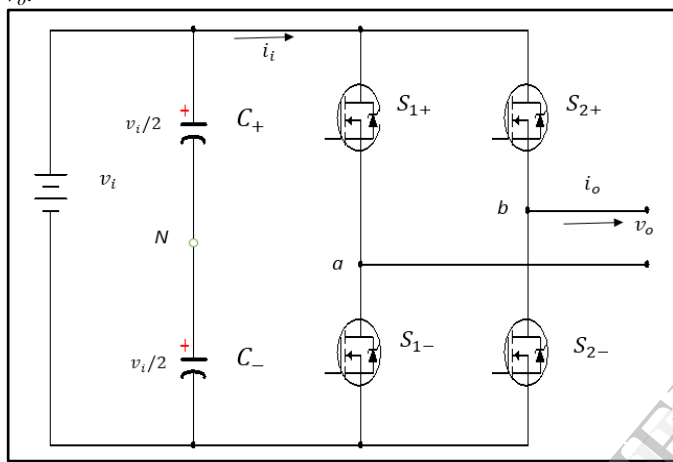


Fig 2 Single-phase full-bridge VSI

TABLE 2 SWITCH STATE FOR A FULL-BRIDGE SINGLE-PHASE VSI

State	State	$v_a$	$v_b$	$v$
$S1_+$ & $S2_-$ are ON & $S1_-$ & $S2_+$ are OFF	1	$v/2$	$-v/2$	$v$
$S1_-$ & $S2_+$ are ON & $S1_+$ & $S2_-$ are OFF	2	$-v/2$	$v/2$	$-v$
$S1_+$ & $S2_+$ are ON & $S1_-$ & $S2_-$ are OFF	3	$v/2$	$v/2$	0
$S1_-$ & $S2_-$ are ON & $S1_+$ & $S2_+$ are OFF	4	$-v/2$	$-v/2$	0
$S1_+$ , $S2_-$ , $S1_-$ & $S2_+$ are OFF	5	$-v/2$ $v/2$	$v/2$ $-v/2$	$-v$ $v$

C. *Three-phase VSI*

Single-phase VSIs cover low-range power applications and three-phase VSIs cover the medium- to high-power applications. The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. The standard three-phase VSI topology is shown in Fig. 3 and the eight valid switch states are given in Table 3.

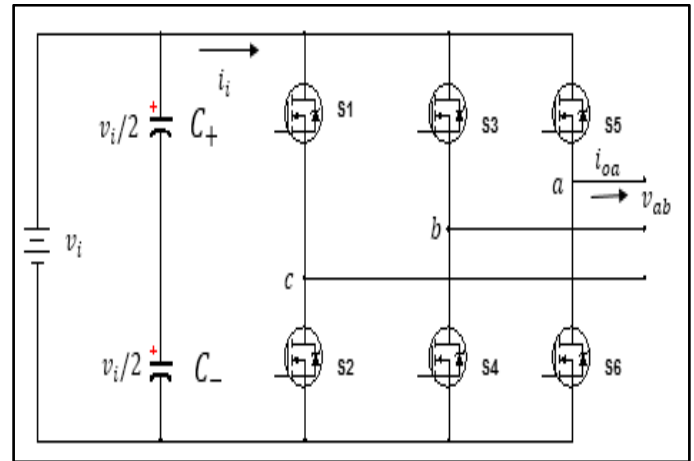


Fig. 3 Three-phase VSI topology

TABLE 3 VALID SWITCH STATES FOR A THREE-PHASE VSI

State	State	$v_{ab}$	$v_b$	$v_a$
$S1, S2,$ and $S6$ are on and $S4, S5,$ and $S3$ are off	1	$v_i$	0	$-v_i$
$S2, S3,$ and $S1$ are on and $S5, S6,$ and $S4$ are off	2	0	$v_i$	$-v_i$
$S3, S4,$ and $S2$ are on and $S6, S1,$ and $S5$ are off	3	$-v_i$	$v_i$	0
$S4, S5,$ and $S3$ are on and $S1, S2,$ and $S6$ are off	4	$-v_i$	0	$v_i$
$S5, S6,$ and $S4$ are on and $S2, S3,$ and $S1$ are off	5	0	$-v_i$	$v_i$
$S6, S1,$ and $S5$ are on and $S3, S4,$ and $S2$ are off	6	$v_i$	$-v_i$	0
$S1, S3,$ and $S5$ are on and $S4, S6,$ and $S2$ are off	7	0	0	0
$S4, S6,$ and $S2$ are on and $S1, S3,$ and $S5$ are off	8	0	0	0

D. *Performance parameters of Inverters*

1) *Harmonic Factor of  $n^{th}$  Harmonic*: The harmonic factor is a measure of the individual harmonic contribution in the output contage of an inveter. It is defined as the ratio of the rms voltage of a particular harmonic component to the rms value of fundamental component.

$$HF_n = \frac{E_{n_{rms}}}{E_{1_{rms}}}$$

2) *Total Harmonic Distortion (THD)*: A total harmonic distortion is a measure of closeness in a shape between the output voltage waveform and its fundamental component. It is defined as the ratio of rms value of the fundamental component.

$$THD = \sqrt{\frac{E_0^2 - E_1^2}{E_1}}$$

3) *Distortion Factor*: A distortion factor indicates the amount of harmonics that remain in the output voltage waveform, after the waveform has been subjected to second-order attenuation. It is defined as

$$DF = \frac{\sqrt{\sum_{n=2,3,\dots}^{\infty} \left(\frac{E_{nrms}}{n^2}\right)^2}}{E_{1rms}}$$

4) *Lowest-Order Harmonics (LOH)*: the lowest frequency harmonic, with a magnitude greater than or equal to 3% of the magnitude of the fundamental component of the output voltage, is known as lowest order harmonic.

In this paper THD is analysed.

### III. PULSE WIDTH MODULATION

Output voltage from an inverter can also be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse-width modulation control used within an inverter. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as Pulse-Width Modulation (PWM) Control.

The advantages possessed by PWM techniques are as under:

- The output voltage control with this method can be obtained without any additional components.
- With the method, lower order harmonics can be eliminated or minimized along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimized.

PWM inverters are quite popular in industrial applications. PWM techniques are characterized by constant amplitude pulses. The width of these pulses is however modulated to obtain inverter output voltage control and to reduce its harmonic content. The different PWM techniques are as under:

- Single-pulse modulation
- Multiple pulse modulation
- Carrier based pulse width modulation(Sinusoidal Pulse Width Modulation)

#### A. Carrier based pulse width modulation

Carrier based pulse width modulation or Sinusoidal Pulse Width Modulation is method in which several pulses per half-cycle are uses. The width of each pulse is varied proportional to the amplitude of a sine-wave. By comparing a sinusoidal reference signal with a triangular carrier wave of frequency  $f_c$ , the gating signals are generated as shown in fig. 4 the reference signal,  $f_r$  determine the inverter output frequency,  $f_o$  and its peak amplitude,  $E_r$  controls the modulation index  $m$ , and then in turn the RMS output voltage  $E_l$ . The

number of pulses per half-cycle depends on the carrier frequency.

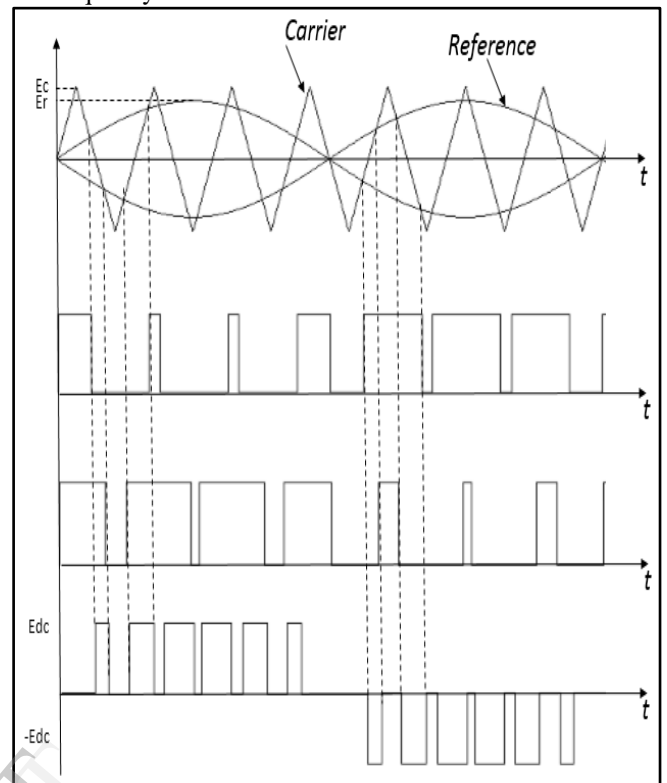


Fig. 4 Sinusoidal Pulse Width Modulation

### IV. HARDWARE DESIGN

#### V. RESULTS

The simulation is done in MATLAB/SIMULINK environment. A Single-phase full bridge inverter using MOSFETs has been tested with gate pulse generated by unipolar Sinusoidal PWM technique. Fig. 5 shows the full bridge inverter and PWM generation scheme.

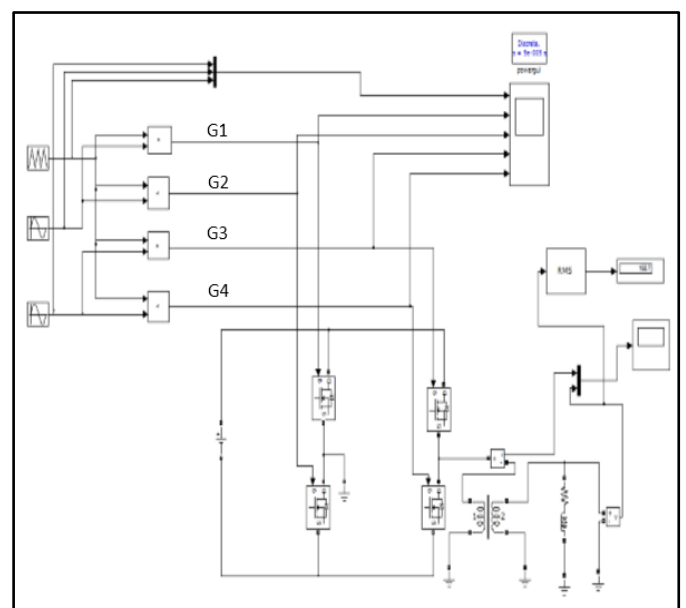


Fig. 5 Full bridge inverter with SPWM

**A. PWM**

Fig. 5 shows PWM generation scheme. Here unipolar PWM configuration is used where a reference sinusoidal signal with frequency 50Hz( $f_r$ ) and magnitude  $E_r$  is compared with carrier triangular signal of frequency 1.02kHz( $f_c$ ) and magnitude  $E_c$ . This scheme produce gate signals G1, G2, G3, and G4. The signal G1 and G2 are generated by comparing triangular signal with sinusoidal with  $0^\circ$  phase shift, G1 and G2 are opposite to each other. Similarly, the signal G3 and G4 are generated by comparing triangular signal with sinusoidal with  $180^\circ$  phase shift, G3 and G4 are opposite to each other.

**B. Single phase full bridge inverter**

Fig. 5 shows single phase full bridge inverter using MOSFETs. 12V Vdc is supplied to the inverter and the output is step up to 230V using step up transformer. RL load is used for testing  $V_{rms}$  and %THD.

Fig. 6 shows the simulate result of the PWM signals and fig. 7 shows the simulated result of inverter output.

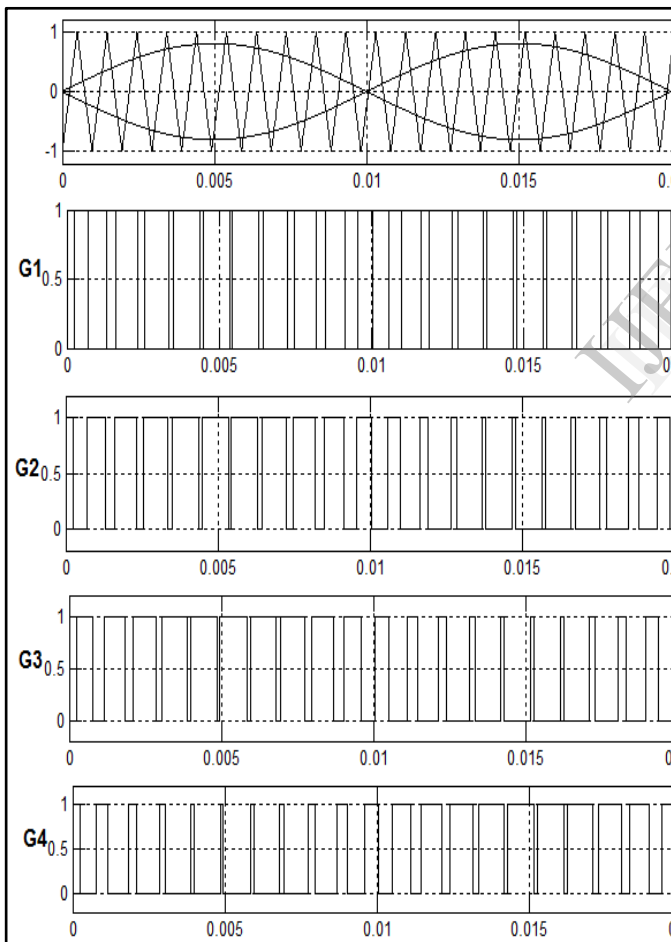


Fig. 6 Sinusoidal PWM

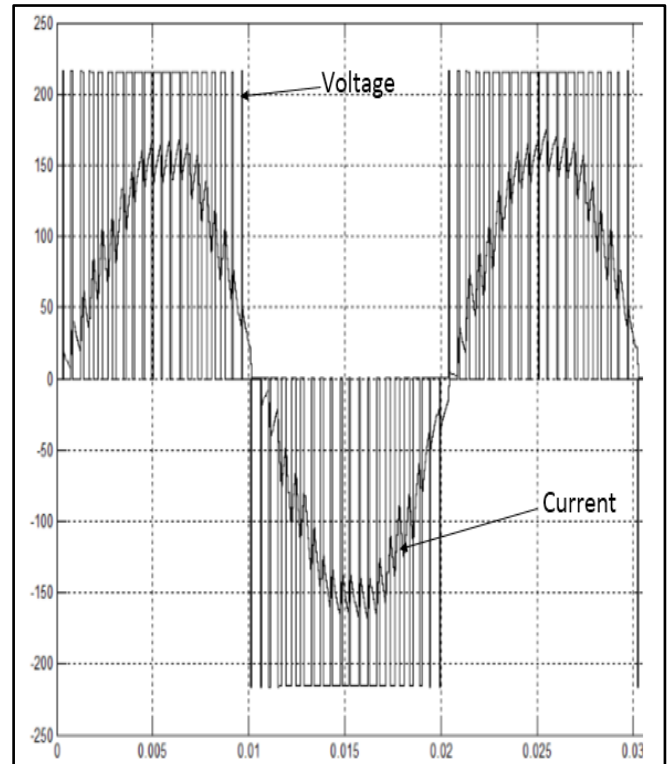


Fig. 7 Output of inverter

As modulation index ( $m$ ) is changed, there is change in output RMS voltage ( $V_{rms}$ ), where,

$$m = \frac{E_c}{E_r}$$

The simulated results for different modulation index are tabulated in Table 4.

TABLE 4 VRMS VALUES

M	Vrms (V)
0.9	175.2
0.8	157.5
0.6	136.2
0.4	110.9
0.2	78.45

From Table 4 it is clear that as the modulation index is lower  $V_{rms}$  is also lowers. This can be used in speed control of AC drives using close loop system. Through feed-back from the load, by proper signal conditioning the modulation index can be varied to get proper  $V_{rms}$ .

Fig. 8 shows %THD (current) of the inverter with RL load,  $R = 15\Omega$ ,  $L = 2e-2$  H

## CONCLUSION

For design of pure sine wave inverter SPWM is better solution. Also by selecting proper value of L better current THD can be observed.

## ACKNOWLEDGMENT

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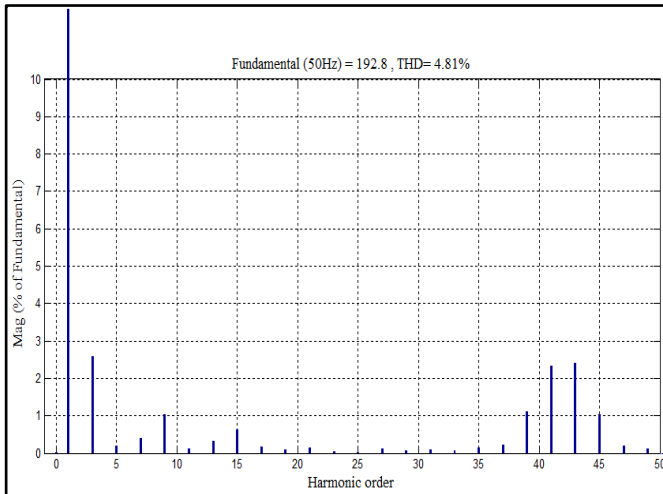


Fig. 8 FFT analysis of full bridge inverter

%THD for reference frequency  $f_r = 50\text{Hz}$  & different carrier frequency  $f_c$ , R, and L are shown in Table 5. From the table it is concluded that for lower value of R & higher value of L gives better THD.

TABLE 5 %THD (CURRENT)

$f_c(\text{kHz})$	$R(\Omega)$	$L(\text{H})$	%THD
1	10	1e-2	6.73
		2e-2	3.96
		3e-2	3.10
	20	1e-2	12.03
		2e-2	6.71
		3e-2	4.86
1.05	10	1e-2	5.99
		2e-2	3.64
		3e-2	2.89
	20	1e-2	10.48
		2e-2	5.97
		3e-2	4.42
2	10	1e-2	5.27
		2e-2	3.10
		3e-2	2.42
	20	1e-2	9.02
		2e-2	5.26
		3e-2	3.82
2.05	10	1e-2	4.84
		2e-2	3.26
		3e-2	2.66
	20	1e-2	7.16
		2e-2	4.84
		3e-2	3.84

[8]