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Study of the Effect of Doping and Body Thickness in a 32 nm Strained-Si on Silicon-Germanium-on-Insulator (SS-SGOI) nMOSFET

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Abstract— **Simulation studies on a strained silicon on silicon-germanium on insulator (SS-SGOI) device has been performed with the powerful Synopsys TCAD tool. The drain current characteristics for various doping concentrations in both the strained silicon layer as well as the virtual SiGe-substrate has been studied. Change in the drain current due to change in body thickness has also been investigated. Additionally, various important device parameters like threshold voltage, off current and drain saturation current have been extracted.**

Keywords—: SS-SGOI nMOSFET, Buried oxide, Virtual substrate, Ultra-thin body

I. INTRODUCTION

Scaling of silicon based MOSFETs has been the driving force for higher integration density, speed and efficiency in microelectronics industry over the last few decades. However, below 90 nm, further scaling down of device dimensions causes various undesirable effects like channel moblty reduction, gate leakage current and other short channel effects. To compensate for these detrimental effects, various new materials have been studied. Strained silicon is one of them due to its improved mobility, high-field velocity and high velocity overshoot of carriers [1].

Strained silicon on insulator (S-SOI) is a promising technology for future generation high speed CMOS devices as it combines both the advantages of enhanced mobility of strained silicon and reduced parasitic capacitance due to the buried oxide (BOX). A number of fabrication processes have been proposed in various research works for developing strained SOI devices [2-5]. Strained silicon on silicon-germanium on insulator (SS-SGOI) is one kind of strained SOI device where SiGe is used as virtual substrate below the silicon channel to make it bi-axially strained [6].

In this paper, we have developed a SS-SGOI device as shown in the figure 1. Device simulations are performed using the powerful Synopsys TCAD tool to study the drain current characteristics for various doping concentrations in both the strained silicon layer and the virtual substrate(SiGe). Change in the drain current behavior due to change in body thickness has also been investigated. Additionally, various important device parameters like threshold voltage, off current and drain saturation current have been extracted.

II. DEVICE STRUCTURE AND BAND DIAGRAM

The device structure to be simulated of 32 nm gate length is shown in figure 1. The structure has been developed using Sentaurus Structure Editor tool-kit. To form the SS-SGOI structure, buried oxide is grown over the Silicon substrate and a thin SiGe-substrate layer is then formed over the BOX followed by a 5 nm thin silicon layer. Due to interfacing of thin Silicon and SiGe, the Si layer gets strained and the effective mass of the electrons decreases due to the strain. Hence a high mobility channel is formed in the strained Si layer. In our study BOX thickness is taken as 100 nm [1], Effective Oxide Thickness (EOT) of the gate oxide is 1.1 nm and aluminum is used as the metal gate.

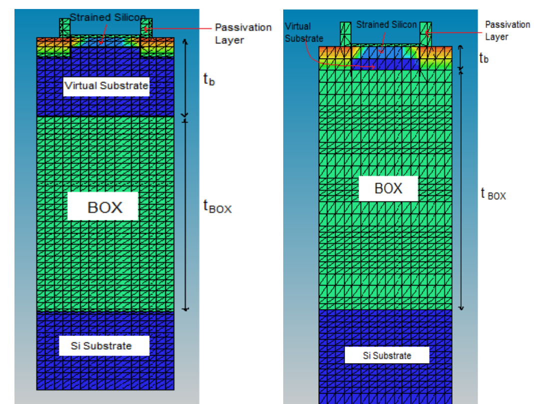

Fig.1. (a) Convensional SS-SGOI nMOSFET structure with t_b ranging from 40nm to 20nm (b) Ultra-thin body SS-SGOI nMOSFET structure with t_b=10nm

Change in band diagram due to strain is shown in figure 2. The tensile biaxial strain on the silicon caused by the lattice mismatch at the s-Si/$Si_{1-x}Ge_x$ interface, leads to a change in the band structure. There are discontinuities at the interface for both the valence and the conduction bands. The electron affinity of silicon increases, the band gap of silicon decreases and the strain leads to the decrease in the effective mass of the electrons. [7].

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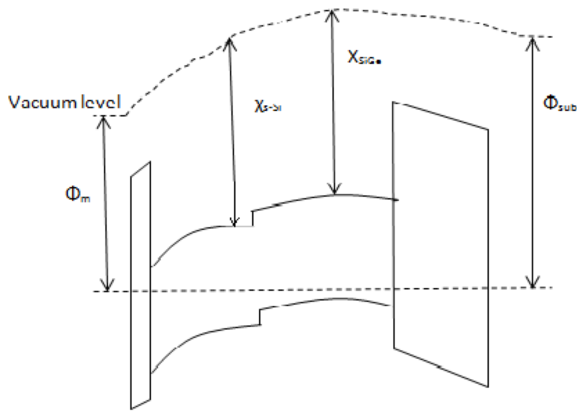

Fig.2. Band Diagram of SS-SGOI Device Structure

The above effects caused by strain can be modeled as [1,7,8]

$$(\Delta E_V)_{s\text{-}Si}=0.74x$$
$$(\Delta E_C)_{s\text{-}Si}=0.57x$$
$$\chi_{s\text{-}Si}=4.17+(\Delta E_C)_{s\text{-}Si}$$
$$(\Delta E_g)_{s\text{-}Si}=0.4x$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s\text{-}Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s\text{-}Si}}\right)^{3/2} \approx 0.075x$$

Where x is the Ge mole fraction in relaxed $Si_{1-x}Ge_x$ layer, $(\Delta E_V)_{s\text{-}Si}$ is the valence band discontinuity at s-Si/$Si_{1-x}Ge_x$ interface, $\chi_{s\text{-}Si}$ is electron affinity of strained silicon, $(\Delta E_C)_{s\text{-}Si}$ is conduction band discontinuity at s-Si/$Si_{1-x}Ge_x$ interface, $(\Delta E_g)_{s\text{-}Si}$ is decrease in band gap of silicon due to strain, V_T is thermal voltage, $N_{V,Si}$ and $N_{V,s\text{-}Si}$ are valence band density of states(DOS) in normal and strained silicon respectively, $m^*_{h,Si}$ and $m^*_{h,s\text{-}Si}$ are hole DOS mass in normal and strained silicon respectively.

The change in band structure of $Si_{1-x}Ge_x$ compared to normal silicon can be expressed as [1]

$(\Delta E_g)_{SiGe}=0.467x$

where $(\Delta E_g)_{SiGe}$ is the decrease in band gap of $Si_{1-x}Ge_x$ from that of normal silicon and x is the Ge mole fraction in $Si_{1-x}Ge_x$.

III. SIMULATION RESULTS AND ANALYSIS

All the device parameters have been extracted and electrical characteristics have been simulated by the powerful Technology Computer Aided Design (TCAD) toolkit of Synopsys called Svisual.

Threshold voltage, ON current and OFF current for various doping concentration and body thickness have been extracted for the ultrathin body strained silicon on SiGe on insulator nMOSFET shown in fig. 1(a) and presented in tabular form below.

TABLE I

Extracted Parameters	Strained Silicon Layer Doping (/cm^3)			
	10^{16}	10^{17}	10^{18}	10^{19}
Threshold Voltage(V)	0.482326	0.483467	0.508792	0.797273
ON Current(mA/um)	1.11769	1.0851	0.92672	0.2351
OFF Current(pA/um)	65.87	44.6	8.02	0.000157

TABLE II

Extracted Parameters	Virtual Substrate (SiGe) Doping (/cm^3)			
	10^{16}	10^{17}	10^{18}	10^{19}
Threshold Voltage(V)	0.479768	0.481288	0.493046	0.589278
ON Current(mA/um)	1.12318	1.11963	1.09048	0.85257
OFF Current(pA/um)	71.4	61.1	23.97	0.0748

From Table I and Table II it is observed that threshold voltage increases due to increase in the doping concentration of strained Si and the virtual SiGe substrate because of increase in the Flat-band voltage. This leads to decrease in the ON current.

The OFF current decreases with increase in doping concentration in the strained silicon layer as well as in the virtual substrate. This is because the OFF current is due to reverse saturation current at the source-substrate and drain substrate reverse biased junctions. If the doping concentration increases, so does the majority carrier concentration. So the minority carrier concentration, which is responsible for the reverse saturation current at the junctions will decrease, thus reducing the OFF current. Further, it is observed that the doping of the strained silicon layer, where the channel is formed at ON state, has a more significant role on the variation of the parameter values compared to virtual substrate doping, especially for higher doping (more than 10^{17} cm^3). This is due to the fact that the Threshold value depends on the Flat-band voltage calculated for the metal-oxide-strained Si interfaces. The doping of the SiGe virtual substrate controls the band-bending profile of the strained Si layer.

TABLE III

Extracted Parameters	Body Thickness			
	40 nm	30 nm	20 nm	10 nm
Threshold Voltage(V)	0.4814 73	0.4750 48	0.4669 22	0.4812 88
ON Current(mA/um)	1.0378 2	1.0302 3	0.9886 05	1.1196 3
OFF Current(pA/um)	1090	2198.9	1377	65.86

From Table III it is observed that the ON current decreases with decrease in body thickness up to 20 nm. However, in case of ultra-thin body where the body thickness is only 10 nm and the buried oxide (BOX) region starts immediately

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after the source and drain region, the ON current suddenly becomes very high. This may be due to the decrease in body-effect coefficient and hence decrease in threshold voltage. The OFF current is also significantly reduced for ultra-thin body SS-SGOI structure as the Source and Drain regions are interfaced with the BOX.

Figures 3 and 4 show I_d Vs V_{ds} and I_d Vs V_{gs} characteristics of ultra-thin body SS-SGOI nMOSFET, respectively for various doping concentrations in strained silicon layer ranging from 10^{16} to 10^{19} /cm^3. Doping concentration in virtual substrate layer is fixed at 10^{17} /cm^3[7]. It is observed that the drain current decreases with increase in doping concentration as threshold voltage increases with increasing doping concentration.

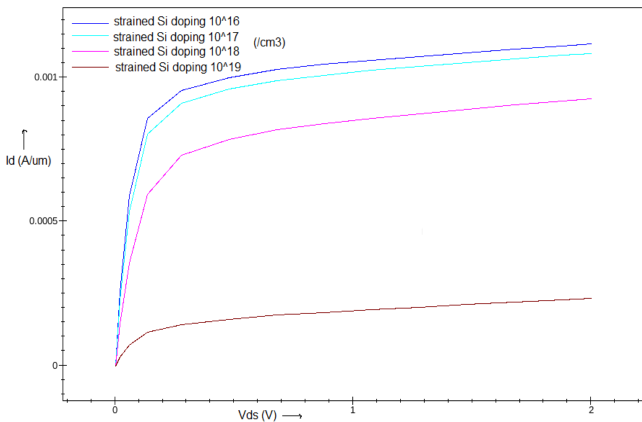

Fig.3. I_d Vs V_{ds} plot for various doping concentrationsin strained silicon layer, gate voltage is 1V

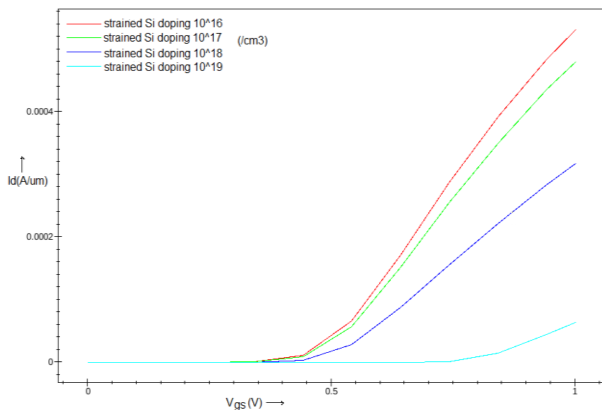

Fig.4. I_d Vs V_{gs} plot for various doping concentrations in strained silicon layer, drain voltage is 50 mV

Figures 5 and 6 show the I_d Vs V_{ds} and I_d Vs V_{gs} characteristics of ultra-thin body SS-SGOI nMOSFET respectively for various doping concentrations in virtual substrate ranging from 10^{16} to 10^{19} /cm^3. The strained silicon layer doping is fixed at 10^{15} /cm^3[7]. It is observed that the drain current decreases with increase in virtual substrate doping.

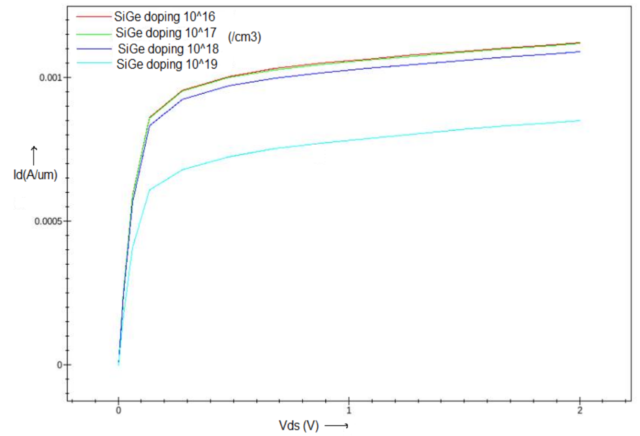

Fig.5. I_d Vs V_{ds} plot for various doping concentrations in virtual substrate (SiGe), gate voltage is 1V

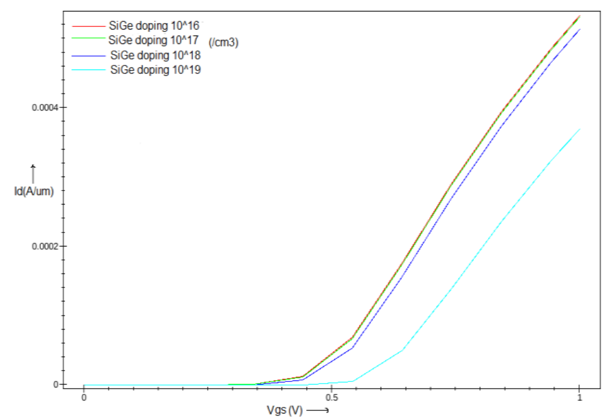

Fig.6. I_d Vs V_{gs} plot for various doping concentrations in virtual substrate (SiGe), drain voltage is 50 mV

Figures 7 and 8 show I_d Vs V_{ds} and I_d Vs V_{gs} characteristics respectively for SGOI nMOSFET of different body thicknesses ranging from 40 nm to 10 nm. Strained silicon layer doping and virtual substrate doping is fixed at 10^{15} /cm^3 and 10^{17}/cm^3. It is observed that drain current slightly decreases with decrease in body thickness up to 20 nm. However, in case of ultra-thin body SGOI structure where the body thickness is 10 nm drain current is significantly high.

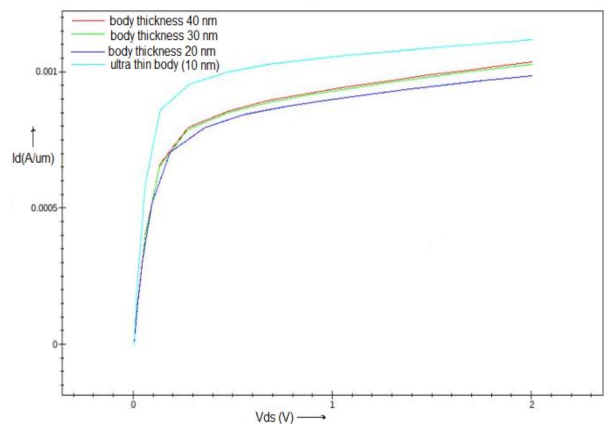

Fig.7. I_d Vs V_{ds} plot for various body thicknesses, gate voltage is 1V

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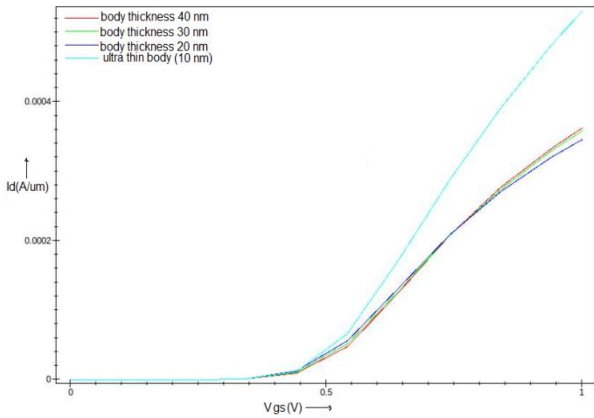

Fig.8. I_d Vs V_{gs} plot for various body thicknesses, drain voltage is 50 mV

Figures 9 and 10 show the subthreshold characteristics of ultra-thin body SS-SGOI nMOSFET for various doping concentrations in strained silicon layer and virtual substrate respectively. It is observed that the drain current of the device at the OFF state is more significantly controlled by strained silicon layer doping compared to virtual substrate doping.

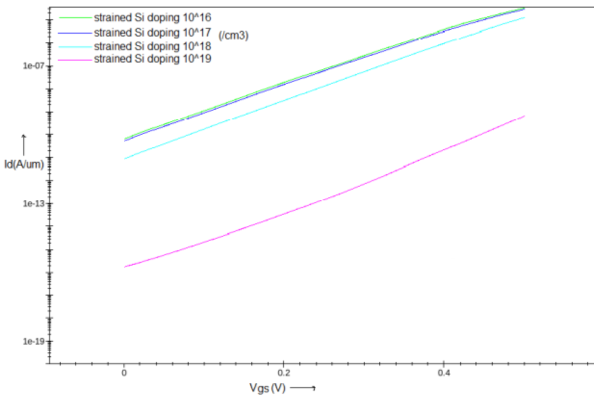

Fig.9. Subthreshold characteristics for various doping concentrations in strained silicon layer, drain voltage 50 mV

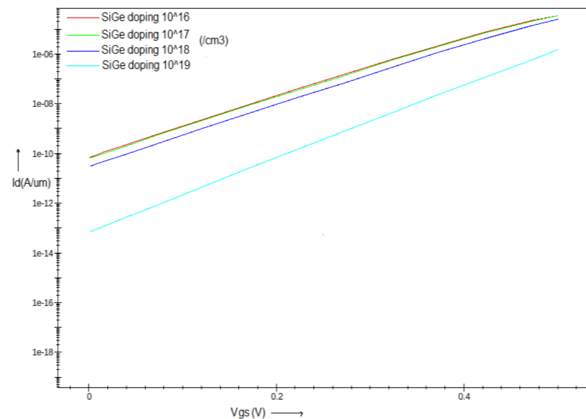

Fig.10. Subthreshold characteristics for various doping concentrations in virtual substrate (SiGe), drain voltage 50 mV

IV. CONCLUSION

A detailed study of 32 nm strained Silicon on Silicon-Germanium on Insulator (SS-SGOI) n-type MOSFET has been performed. All the electrical characterizations and parameter extractions have been done using powerful Synopsys TCAD tool-kit. It is found that changes in Threshold voltage, ON current and OFF current is controlled more by strained silicon layer doping where the channel is formed than that of virtual substrate (SiGe). Although ON current decreases with decreasing body thickness, it suddenly increases significantly for ultra-thin body (body thickness 10 nm). OFF current of ultra-thin body SS-SGOI is also quite less.

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REFERENCES

[1] Vivek Venkataraman, Susheel Nawal, and M. Jagadesh Kumar, "Compact Analytical Threshold-Voltage Model of Nanoscale Fully Depleted Strained-Si on Silicon–Germanium-on-Insulator (SGOI) MOSFETs" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 3, MARCH 2007, pp. 554-562.

[2] P. Mei and Y. C. Yeo, "Strained silicon substrate technologies for enhancement of transistor performance," *J. Ceram. Process. Res.*, vol. 5, no. 3, pp. 261–263, 2004.

[3] H. Z. Yin, K. D. Hobart, R. L. Peterson, F. J. Kum, and J. C. Stur, "Ultrathin strained-SOI by stress balance on compliant substrates and FET performance," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2207– 2214, Oct. 2005.

[4] S. Takagi, N. Sugiyama, T. Mizuno, T. Tezuka, and A. Kurobe, "Device structure and electrical characteristics of strained-Si-on-insulator (strained-SOI) MOSFETs," *Mater. Sci. Eng., B, Solid-State Mater. Adv. Technol.*, vol. 89, no. 1–3, pp. 426–434, Feb. 2002.

[5] S. Takagi, T. Mizuno, T. Tezuka, N. Sugiyama, T. Numata, K. Usuda, Y. Moriyama, S. Nakaharai, J. Koga, A. Tanabe, and T. Maeda, "Fabrication and device characteristics of strained-Si-on-insulator (strained-SOI) CMOS," *Appl. Surf. Sci.*, vol. 224, no. 1–4, pp. 241–247, Mar. 2004.

[6] F. Gamiz, P. C. Cassinello, J. B. Roldan, and F. J. Molinos, "Electron transport in strained Si inversion layers grown on SiGe-on-insulator substrates," *J. Appl. Phys.*, vol. 92, no. 1, pp. 288–295, Jul. 2002.

[7] J. C. Tinoco, J. Alvarado, A. G. Martinez-Lopez, B. Iñiguez, and A. Cerdeira, "Drain Current Model for Bulk Strained Silicon NMOSFETs" Proc. of 8th International Caribbean Conference on Devices, Circuts and Systems (ICCDCS), March 2012, pp. 1-4.

[8] J C Tinoco, R Garcia, B Γniguez, A Cerdeira and M Estrada, "Threshold voltage model for bulk strained-silicon NMOSFETs" Semicond. Sci. Technol. **23** (2008) 035017 (5pp)

[9] Wong Yah Jin, Ismail Saad and Razali Ismail, "Characterization of Strained Silicon MOSFET Using Semiconductor TCAD Tools" Semiconductor Electronics, 2006. ICSE '06. IEEE International Conference,pp.924-927.

[10] Toufik Sadi, Robert W. Kelsall, and Neil J. Pilgrim, "Electrothermal Monte Carlo Simulation of Submicrometer Si/SiGe MODFETs" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 2, FEBRUARY 2007, pp. 332-339.

[11] Tejas Krishnamohan, Zoran Krivokapic, Ken Uchida, Yoshio Nishi, and Krishna C. Saraswat, "High-Mobility Ultrathin Strained Ge MOSFETs on Bulk and SOI With Low Band-to-Band Tunneling Leakage: Experiments" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 5, MAY 2006, pp. 990-999.

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