Swarm Based Approach for the Optimization of Power-Delay Product in a CMOS Repeater Driven RC Interconnect Line

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Abstract

In this work, Particle Swarm Optimization technique has been implemented in a CMOS repeater driven RC interconnect line for Power delay product minimization. The work aims at minimizing the delays associated with the RC parasitics at 180nm technology and hence optimizing power delay product.Different researchers have proposed different techniques to reduce the interconnect delay. However, the most effective technique for delay reduction is to insert buffers in between the RC interconnects for driving large interconnect loads. Although inserting repeaters reduces overall delay but if the number of repeaters inserted in the repeater chain is not optimal it may lead to increase in delay and power dissipation. So there is a need to optimize various parameters such as number of repeaters, size of repeaters and applied voltage. In this work, a factor called Power Delay Product has been optimized using the evolutionary technique popularly known as particle swarm optimization. The simulations are also carried out using CADENCE SPECTRE tool at 180 nm technology andthe results are finally compared with those obtained using PSO simulation in MATLAB.

Keywords **–** Interconnects, Repeaters, Optimize, Lumped, Power-Delay Product

1. Introduction

In recent years, the size of complementary metal–oxide–semiconductor (CMOS) integrated circuits continues to decrease. As we move into deep submicron technology, the long interconnect delay have become common on chip feature. As a result wire delaysdominate over gate delays. With a linear increase in length, interconnect delay increases quadratically due to a linear increase in both interconnect resistance and capacitance [1], [2]. Also, large interconnect loads not only affect circuit performance, but also degrades the waveform shape and causes excessive short-circuit power to be dissipated in the stage loading a CMOS logic gate, filters, etc.

Interconnect delay is the combined effect of parasitic resistance, capacitance and inductance associated with it. Each of these parasitic elements increase linearly with the interconnect length. This increase in the interconnect parameters mainly occurs when feature sizes enter the nanometer era. Many design techniques have therefore been developed to minimize the propagation delay of global interconnect. Repeaters are often used to minimize the delay to propagate a signal through those interconnect lines that are best modeled as an *RC* impedance.But the number of repeaters plays a key role in deciding the overall delay of the repeater loaded interconnects. If optimal number of repeaters is not used in the repeater chain then this tends to increase in delay. Moreover as the number of repeaters in a chain increases the power dissipation also increases.So the aim is to optimize the number of repeaters to have minimum interconnect delay. Other factors namely size of repeater and applied voltage are also responsible for increasing RC interconnect delays. So there should be some optimal value of all these factors to have minimum delay and power so that the factor called power-delay product has been optimized.

2. Lumped RC Interconnect Model

The electrical properties of the interconnect wire mainly includes three parameters namely capacitance, resistance, and inductance. These parasitic elements have an impact on the electrical behavior of the circuit and influence its delay, power dissipation, and reliability.In this paper interconnects having RC parasitic element with a simple L-shaped model is considered [3].

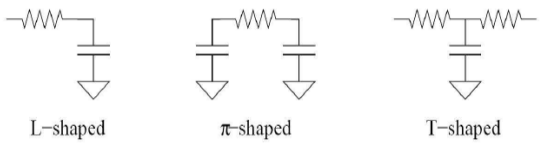

Figure 1. Interconnect RC models

RC delays should only be considered when the rise (fall) time at the line input is smaller than *RC*, the rise (fall) time of the line. When this condition is not met, the change in signal is slower than the propagation delay of the wire, and a lumped capacitive model suffices.

3. Interconnect Delay Reduction using Repeaters

With the continued scaling of process technology, the interconnect resistance per unit length continues to increase, the capacitance per unit length remains roughly constant and logic delay continues to decrease. These trends have caused interconnect delay to become more dominant than logic delay. Interconnect-driven timing optimization techniques, such as wire sizing, buffer insertion and gate sizing have gained widespread acceptance in deep submicron design. In particular, buffer insertion techniques have been successful in reducing interconnect delay. To the first order, interconnect delay is proportional to the square of the length of the wire. Inserting buffers effectively divides the wire into smaller segments, which makes the interconnect delay almost linear in terms of length (plus the buffer delays). Many design techniques have therefore been developed to minimize the propagation delay of global interconnect. Repeaters are often used to minimize the delay to propagate a signal through those interconnect lines that are best modeled as an *RC* impedance. Since the delay of a long unbuffered line is quadratic in its length, long interconnects are divided into a number of segments with repeaters or buffers. [4]. So the most popular design approach to reduce the propagation delay of long wires is to introduce intermediate buffers, also called repeaters, in the interconnect line.

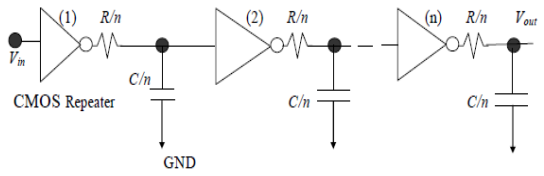

Figure 2.RC interconnect model having n repeaters[5]

Figure 2.shows the equivalent circuit of a repeater driven interconnect, where a number of equal sized repeaters are inserted along an interconnect. When *n* number of uniform repeaters are inserted in between, the interconnect capacitance (*C*/*n*) of the subsection comes in parallel with repeater capacitance (C_{rep}).

In this work, the resistive interconnect is considered which is modeled as a lumped RC load having resistance R=1KΩ and capacitance C=1pF. In order to optimize the number of repeaters for having minimum delay, t_{90}% delay has been calculated by inserting repeater in between the RC interconnect model. Figure 3 shows the long interconnect having RC parasitics with the six repeaters inserted in between them. The delay of the repeater loaded interconnect is calculated by varying supply voltage and number of repeaters.

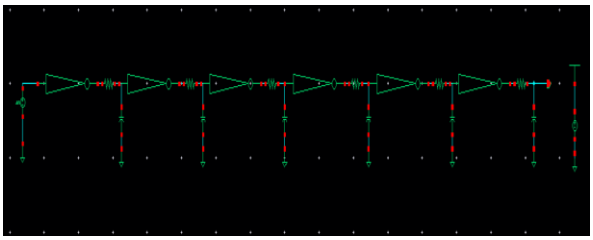

Figure 3. RC interconnect with six repeaters

Since delay also depends on the supply voltage $V_{DD}$and width of transistor W_n,so for each repeater insertion, delay has been calculated for a set of V_{DD} at particular W_n (MOS width). Moreover two transistor technologies has been considered one at W_p = 3µm; W_n = 1µm and other at W_p = 1.8µm; W_n = 0.6µm

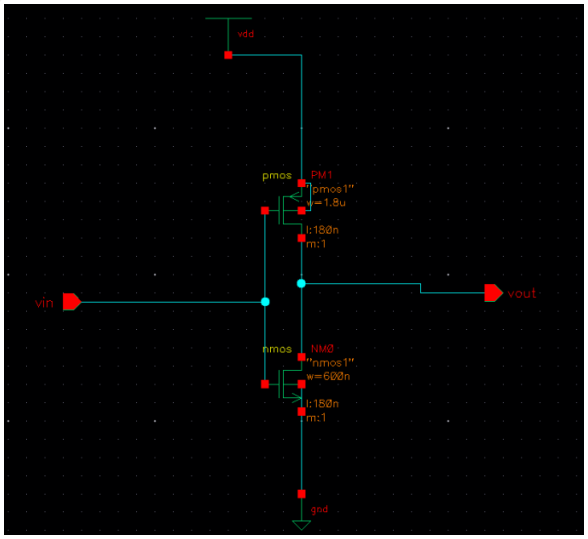

Figure 4. CMOS inverter with W_p = 1.8µm; W_n = 0.6µm

After calculating the t_{90}% for a set of repeaters, readings have been analyzed for minimal delay with respect to voltage and technology.

The analytical expression for ninety percent delay ($t_{90\%}$) of a repeater loaded RC interconnect is given by [6], [7], [8]:

$$t_{90\%} = \left(\frac{n-1}{2}\right)\left[\left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right) ln\left(\frac{V_{DD} - |V_{tp}|}{V_{tn}}\right) + \left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right)\left|ln\left(\frac{V_{tn}}{V_{DD} - |V_{tp}|}\right)\right|\right] + 2.3\left(\frac{1}{G_{don}} + \frac{R}{n}\right)\frac{C}{n} \quad (1)$$

Similarly the expression for even number of repeaters is:

$$t_{90\%} = \left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right) ln\left(\frac{V_{DD}}{V_{tn}}\right) + \frac{n-2}{2} X \left[\left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right) ln\left(\frac{V_{DD} - |V_{tp}|}{V_{tn}}\right) + \left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right)\left|ln\left(\frac{V_{tn}}{V_{DD} - |V_{tp}|}\right)\right|\right] + 2.3\left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n}\right) - \left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right) ln\left(\frac{V_{DD}}{V_{DD} - |V_{tp}|}\right) \quad (2)$$

The above delay expression is dependent on saturation drain conductance where $G_{don}$and $G_{dop}$are defined for NMOS and PMOS respectively. Here V_{DD} is supply voltage, $C_{rep}$is repeater capacitance and n is number of repeaters. But it has also been found that $G_{don/p}$ and C_{rep}also depend on supply voltage and width of transistors ($W_{n/p}$)

The dependence of G_{don}, G_{dop} and C_{rep} on V_{DD}, W_n is given by following expressions

$G_{don} = 0.5\ (W_n)^{0.95}(V_{DD})^{1.29}$(inmS)
$C_{rep} = 85.78\ (W_n)^{0.575}(V_{DD})^{-0.612}$ (infF)
$G_{dop} = 0.47\ (W_n)^{1.05}(V_{DD})^{1.51}$ (inmS)

After substituting the values of G_{don}, $G_{dop}$and C_{rep}in equation 1, the expression for delay is in terms of V_{DD}, W_n and n has been obtained.

4. Power Minimization

In this work power analysis of repeater loaded interconnects is also carried out. Today due to high integration densities and high speeds in VLSI circuit's power dissipation is a prime criterion. The total power dissipation includes dynamic power, short circuit power and static power dissipation (leakage). In long interconnects dynamic (switching) power and short circuit power is appreciably large as compared to leakage power.
Thus the total power dissipation in interconnect is equal to the sum of dynamic power, short circuit power and the leakage power. The expression is given by [4]:

$$P_{repeater} = P_{switching} + P_{short-circuit} + P_{leakage}$$

Since this work is based on long interconnects the static power dissipation can be neglected for 180nm technology [9].
There are three power dissipation mechanisms:
Dynamic Power: It is the power consumed due to charging and discharging the load capacitance. Dynamic power has been well studied and is characterized by the following well-known expression:

$$P_d = \alpha f C_L V_{DD}^2$$

Here f is the clock frequency, V_{DD} is supply voltage and α is the switching factor (here α= 1).

In the repeater loaded RC interconnect the dynamic power is given by the expression

$$P_d = \alpha f (C + nC_{rep}) V_{DD}^2$$

Short Circuit Power: This is the power consumed when the signal applied at the input of a CMOS inverter has a finite slew rate, a direct current path exists between V_{DD} and the ground when the input signal switches between V_{tn} and $V_{DD}+V_{tp.}$ It is a function of input transition time, output load capacitance and the size of transistor [4]

$$P_{sc} = \alpha t_r V_{DD} I_{sc} W_n f$$

Here I_{sc} is the short circuit current.

Leakage Power: The leakage current comprises of Sub-threshold current and gate leakage current.

$$P_{leakage} = V_{DD} I_{Leakage}$$

where V_{DD} is supply voltage and $I_{Leakage}$ is leakage current.

Therefore the total power in this case is written as the sum of dynamic and short circuit power:

$$P_{diss} = \alpha t_r (C + nC_{rep}) + \alpha t_r V_{DD} I_{sc} W_n f \quad (3)$$

The variation in the number of repeaters is also been done required to minimize the delay and power. Total power dissipation is obtained using transient analysis. The simulations are carried out using Cadence Virtuoso tool.

5. Power-Delay Product

The power-delay product is a fundamental parameter which is often used for measuring the quality and the performance of a CMOS process and gate designs. As a physical quantity, the power-delay product can be interpreted in the average energy required for a gate to switch its output voltage from low to high and from high to low[10].
At 180nm technology, leakage power can be neglected so in this work dynamic power and short circuit power are considered. As a trade-off between power and delay is required so this work aims at finding the optimum number of repeaters at which the product of power and delay is minimum.
Mathematically, PDP can be formulated as

*PDP = power * Delay*

Now using equations of power (3) and delay(1 or 2) above PDP has been obtained.

$$PDP = \left(\left(\frac{n-1}{2}\right)\left[\left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right) ln\left(\frac{V_{DD} - |V_{tp}|}{V_{tn}}\right) + \left(\frac{1}{G_{don}} + \frac{R}{n}\right)\left(\frac{C}{n} + C_{rep}\right)\left| ln\left(\frac{V_{tn}}{V_{DD} - |V_{tp}|}\right)\right|\right] + 2.3\left(\frac{1}{G_{don}} + \frac{R}{n}\right)\frac{C}{n}\right)(\alpha t_r (C + nC_{rep}) + \alpha t_r V_{DD} I_{sc} W_n f \quad (4)$$

This is the final analytical expression of power–delay product that is to be optimized for three variables namely number of repeaters, supply voltage and transistor width.

6. Optimization using Particle Swarm Technique

The problem of interconnect optimization can be also solved using evolutionary algorithms. Recently these algorithms are gaining popularity for solving optimization problems in the various fields like antenna, controllers, digital signal processing etc. VLSI is also one such field in which optimization problems can be effectively solved using these algorithms, taking lesser time as compared to the traditional simulation techniques. Kennedy and Eberhart (1995) proposed an approach called "Particle Swarm Optimization" which is inspired from the choreography of a bird flock[11]. The idea of this approach is to simulate the movements of a group (Population) of birds which aim to find food. The approach can be seen as a distributed behavioral algorithm that performs multidimensional search. In the simulation, the behavior of each individual is affected by either the best local (i.e. within a certain neighborhood) or the best global individual. The approach uses then the concept of population and a measure of performance similar to the fitness value used with evolutionary algorithm.
The PSO algorithm consists of just three steps, which are repeated until some stopping condition is met.

1) Evaluate the fitness of each particle
2) Update individual and global best fitnesses and positions
3) Update velocity and position of each particle

The first two steps are fairly trivial. Fitness evaluation is conducted by supplying the candidate solution to the objective function. Individual and global best fitnesses and positions are updated by comparing the newly evaluated fitnesses against the previous individual and global best fitnesses, and replacing the best fitnesses and positions as necessary.The velocity and position update step is responsible for the optimization ability of the PSO algorithm.
The velocity of each particle in the swarm is updated using the following equation:

$$v_i(t+1) = wv_i(t) + c_1 r_1[x(t) - x_i(t)] + c_2 r_2[g(t) - x_i(t)]$$

The parameters w, c_1, and c_2 ($0 \le w \le 1.2$, $0 \le c_1 \le 2$, and $0 \le c_2 \le 2$) are user-supplied coefficients. The values r_1 and r_2 ($0 \le r1 \le 1$ and $0 \le r2 \le 1$) are random values regenerated for each velocity update.

Once the velocity for each particle is calculated, each particle's position is updated by applying the new velocity to the particle's previous position:

$$x_i(t+1) = x_i(t) + v_i(t+1)$$

This process is repeated until some stopping condition is met. Some common stopping conditions include: a preset number of iterations of the PSO algorithm, a number of iterations since the last update of the global best candidate solution, or a predefined target fitness value.

In this work, the main objective is to optimize the Power Delay Product (PDP). As it has been already discussed that delay in repeater loaded RC interconnects is minimized using repeater insertion technique but non optimal number of repeaters inserted in a chain sometimes leads to excessive power dissipation, so a trade-off is required between delay and power such that delay is also minimized while keeping power dissipation in control. Therefore for obtaining minimal PDP and optimizing the number of repeaters, NMOS width and power supply, here particle swarm optimization technique has been implemented in MATLAB Tool. Power-delay product is the objective function obtained using equation (4) and the algorithm aims at minimizing the PDP value.

6. Simulation Results

The optimal interconnect design problem is solved using particle swarm optimization and the results thus obtained are verified using Cadence Spectre simulator at 180 nm technology.The device has been implemented with transistor channel width of W_p = 3µm; W_n = 1µm (here $W_p \cong 3W_n$) and channel lengths of $L_n = L_p$ = 0.18µm. (where the subscripts n and p refer to NMOS and PMOS respectively).In this work, a voltage step of magnitude equal to the CMOS supply voltage is applied at the input of first repeater. Here the input is in the form of a symmetric voltage pulse and the input bit rate is $5x10^7$bps (f= 50MHz, 20ns is the time period of the pulse). Firstly the simulation readings using cadence spectre tool at 180nm has been obtained.

Table 1 and table 2 shows the effect of voltage on time delay($t_{90\%}$) at two transistor widths. The results shown below depicts the variation in the time delay with the increasing number of repeaters with the scaling of voltage .The results show that with scaling of voltage the value of delay increases. For instance, for V_{DD} = 1.8V, the delay obtained for n = 1 is 4.89ns for W_n = 3µm while for W_n = 1.8µm it is equal to 6.89ns. So as the transistor width is reduced the time delay increases.

Table 1. Variation in ninety percent ($t_{90\%}$) time delay (ns) with respect to change in number of Repeaters and Change in supply voltage for W_p = 3µm; W_n = 1µm

V_{DD} (V) / Repeaters	1.8	1.6	1.5	1.4	1.2	1
1	4.89	5.3	5.56	5.88	5.99	-
2	3.08	3.43	3.68	4	4.972	6.89
3	3.01	3.37	3.63	3.95	4.94	6.98
4	2.57	2.94	3.19	3.50	4.50	**6.54**
5	2.8	3.17	3.40	**3.43**	**4.44**	6.8
6	**2.47**	**2.85**	**3.09**	3.88	4.72	6.54
7	2.75	3.13	3.39	3.43	4.47	6.89
8	2.48	2.85	3.11	3.75	4.76	6.62
9	2.77	3.16	3.41	3.48	4.545	6.9
10	2.49	2.88	3.15	3.70	4.74	6.75

Table 2. Variation in ninety percent ($t_{90\%}$) time delay (ns) with respect to change in number of Repeaters and Change in supply voltage for W_p = 1.8µm; W_n = 0.6µm

V_{DD}(V) / Repeaters	1.8	1.6	1.5	1.4	1.2	1
1	6.89	7.45	7.93	8.95	10.73	-
2	4.78	5.33	5.68	6.21	7.67	9.94
3	4.64	5.13	5.52	6.07	7.58	10.7
4	4.08	4.62	5.02	5.50	6.98	9.98
5	4.27	4.84	5.23	5.73	7.23	10.31
6	3.93	4.47	5.04	5.8	6.94	**9.90**
7	4.2	4.76	5.1	**5.32**	**6.84**	10.24
8	**3.89**	**4.44**	**4.82**	5.62	7.14	9.94
9	4.19	4.75	5.13	5.34	6.87	10.27
10	3.89	4.45	4.84	5.51	7.06	10.05

From table 1, the minimum time delay obtained is 2.47 ns at V_{DD} = 1.8V, the optimum number of repeaters is n = 6 and as the voltage is scaled down the optimum

number of repeaters gradually decreases. Similarly from table 2 the optimized number of repeaters comes out to be 8 at V_{DD} = 1.8V with corresponding minimum time delay of 3.89 ns.

After finding the optimized number of repeaters for minimum time delay at different voltages the corresponding power dissipated is calculated and hence power-delay product has been obtained for both transistor widths.

Table 3. Variation in Power Delay Product (PDP) with change in supply voltage for W_p = 3µm; W_n = 1µm

Supply Voltage V_{DD} (Volts)	Optimum Number of Repeaters (n_o)	Optimum Time Delay (ns)	Power Dissipated (µW)	Power Delay Product (µW- ns)
1.8	6	2.47	182	449.54
1.6	6	2.85	141	401.85
1.5	6	3.09	123	380.07
1.4	5	3.43	105.6	362.20
1.2	5	4.44	77.17	**342.63**
1	4	6.54	52.7	344.65

Table 4. Variation in Power Delay Product (PDP) with change in supply voltage for W_p = 1.8µm; W_n = 0.6µm

Supply voltage V_{DD} (Volts)	Optimum number of repeaters (n_o)	Optimum time delay (ns)	Power Dissipated(µW)	Power delay Product (µW- ns)
1.8	8	3.89	179.2	697.08
1.6	8	4.44	139.7	620.26
1.5	8	4.82	122.2	589.00
1.4	7	5.32	105.9	563.38
1.2	7	6.84	77.31	**528.80**
1	6	9.90	56.36	557.96

Table 3 & 4 depicts as the voltage has been scaled down the corresponding PDP value also decreases until 1.2V.From the readings, the optimized PDP value is 342.63µW- ns at optimized repeaters n_o = 5, voltage V_{DD} = 1.2V and W_n = 1µm with a time delay of 4.44 ns.

In order to implement particle swarm optimization technique equation 4 has been taken as the objective function. The different PSO parameters has been set and then optimized PDP value is obtained with corresponding values of optimized number of repeaters, supply voltage (V_{DD}) and CMOS transistor width (W_n).

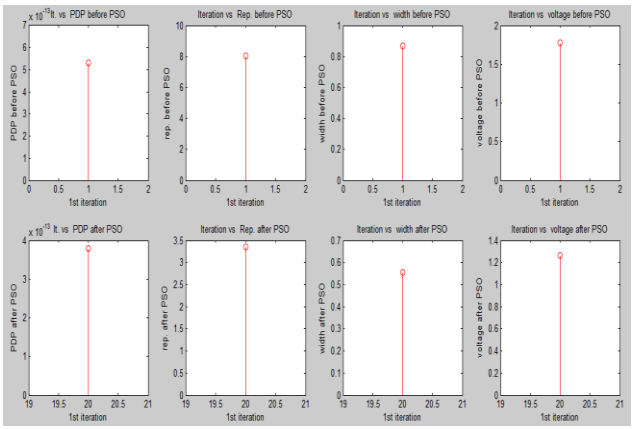

Figure5. PSO based results for power delay product of *RC* interconnect for even number of repeaters at180nm technology.

The results show that the before applying PSO, the power delay product is 5.317×10^{-13}Ws at n_o= 8, W_{no}= 0.868 µm and optimum V_{DD}= 1.78V. But the results obtained after applying PSO are optimized values with power delay product = 3.798×10^{-13}Ws at n_o= 3.35 (approx. 3), W_{no}= 0.55 µm and optimum V_{DD}= 1.26V.

Table below gives the comparison between the PSO results and those obtained using Cadence simulation.

Table 5. Results Obtained by Cadence Simulations&PSO,for Optimal Interconnect Design for Minimum PDP at 180nm technology

Simulation technique	Optimal number of repeaters (n_o)	V_{DD} (Volts)	Optimal Size of Repeaters, W_{no} (in µm)	PDP ($x10^{-13}$ in Ws)
Cadence	5	1.2	1µm	3.42
PSO	3.35~3	1.26	0.55µm	3.79

Table 5 shows that the results of particle swarm optimization are in in close deal with the Cadence results. The time required for solving the problem using PSO has been tremendous when compared with

the timing of the simulation technique. Thus the algorithm used has been very useful in solving complex optimization problems which otherwise take longer time when solved using traditional simulation techniques.

7. Conclusion

The particle swarm optimization technique has been successfully implemented to find the optimum power-delay product at optimized number of repeaters, supply voltage $V_{DD}$and CMOS transistor width (W_n). The simulation results obtained using Cadence spectre tool are in good agreement with the results obtained using particle swarm optimization technique in Matlab. The percentage error between the two results for power-delay product comes out to be 9.7%. The results obtained for power-delay product using cadence simulation attain minimum value at low voltage of V_{DD}i.e 1.2V for both transistor widths and beyond this value the power-delay product increases as $V_{DD}$is increased.

The particle swarm optimization technique has proved to be a efficient technique in getting simultaneously both the optimal values of power-delay product and repeater variables.

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