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# Switching Power Reduction Technique for Turbo Decoders

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*Abstract* – In wireless communications Turbo codes play an important role among other application domains. A decoder of these codes is typically the most power intensive component in the processing chain of a wireless receiver. The decoders iterative nature decoders represents a dynamic workload. This presents a dynamic power management policy for these decoders. According to a prediction of the workload involved within the decoding task an algorithm is proposed to manage the power of the decoder. when operating the decoder at a high power mode, the proposed algorithm looks for opportunities to switch to a lower power mode that guarantees for the task completion. We apply this technique to an Turbo decoder and explore the feasibility of a VLSI implementation on a CMOS technology. Energy savings of up to 54% were achieved in error-correction performance with low loss.

*Index Terms* - Dynamic power management, iterative decoding, low-density parity-check (LDPC) codes, low power design, turbo codes.



## I. INTRODUCTION

For modern capacity the iterative decoding techniques are currently dominating the choices for forward error correction (FEC).Turbo codes, was proposed in 1993, these codes approach the Shannon capacity limit triggered the breakthrough in channel coding techniques. This was followed the rediscovery of low-density parity-check (LDPC) codes in the 1990's, proposed by Gallager in 1963.

In Modern wireless communication ,they have already adopted these types of codes for FEC and channel coding applications.For example, Turbo codes are mainly used in the 3GPP Universal Mobile Telecommunications System (UMTS) and its long term evolution (LTE) system.

Turbo codes are decoded by an iterative message-passing algorithm. Iterations are executed until a stopping criterion is satisfied or a maximum number of iterations is reached. The power of the decoders can be reduced due to the iterative nature of the docoders.In earlier ,Iteration control techniques are also used to reduce the operational complexity of the decoder through the detection of codeblock convergence.

Through this work, we can reduce the problem of power consumption in decoders based upon the following observations.

• Mostly,Practical decoders are designed to execute a maximum number of iterations in order to achieve the timing deadline.

• Error-free decoding can be achieved with a few iterations under good channel conditions.

• A codeblock might not even be decoded with the maximum number of iterations under bad channel conditions.

By monitoring the dynamics of the decoding process it is possible to control a power manageable decoder with increase in energy efficiency. The proposed policy continuously looks for opportunities to slowdown the system and to reclaim the timing slack due to a codeblock ,converges before the task deadline. Based upon the workload prediction of the decoder, we take advantage that the decoder is designed for a maximum number of iterations to takes place within a particular timing deadline. We propose an online algorithm that adjusts the operation mode of a decoder depends upon the characteristic behavior of a convergence metric. In addition to that, we explore the feasibility of a VLSI implementation on a CMOS technology of 65 nm for an LTE Turbo decoder. our work deals with dynamic power management for LDPC decoders was presented.

In Section II the targeted codes are introduced. In Section III, a flow chart will explains about dynamic power management and the proposed control policy. Section IV outlines the hardware implementation of the proposed control technique with results based on the performance, policy tuning and obtained energy savings. The achieved energy savings are compared with similar works. Section V will concludes this paper.

## II. TURBO CODES

In Turbo codes ,the parallel concatenation of two convolutional encoders separated by an interleaver. The decoding nature of these codes consists of the decoding of the individual convolutional component codes and the informations are exchanged iteratively. Soft-input soft-output (SISO) decoders are used and execute the maximum a posteriori(MAP) algorithm in the logarithmic domain. The general structure of a Turbo decoder is shown in Fig. 1. Intrinsic messages ($\delta_s$ for systematic bits and $\delta_{p1,p2}$ for parity bits)are in the form of log-likelihood ratios (LLR) which are distributed in non-interleaved/interleaved form to two MAP decoders.In MAP unit, each decoding round is performed by a half-iteration. Iterations are performed until convergence is achieved or a maximum number of iterations is completed.

In the following, by monitoring the dynamics of the decoding process it should be possible to predict decoder workload.The term workload to refer to either iterations or half-iterations.

## III. DYNAMIC POWER MANAGEMENT

The Dynamic power management (DPM) refers to a set of techniques to achieve energy-efficient operation of a system. This is performed by reconfiguring the system to provide a requested service and performance level with a minimum energy based upon run-time observations. Several techniques are used to achieve this at different levels such as sleep, slowdown modes and clock gating. To apply DPM usually two premises are considered: the system experiences a non-uniform workload during operation-time and it is possible to predict the fluctuations of the workload. Generally, a power manager executes a control procedure known as policy based upon observations of the task workload.

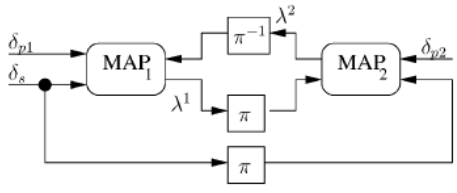



Fig. 1. General structure of a Turbo decoder.

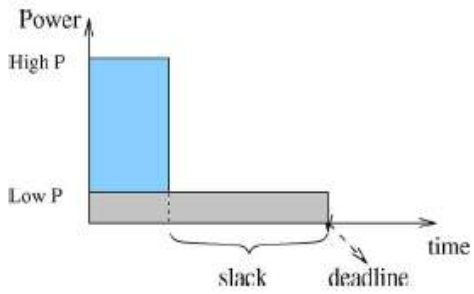



Fig. 2. Example power/slowdown scenario.

The number of iterations in the decoder depends upon the reliability of the decoding process. It is determined by the level of noise in the received codeblock. Typically, the decoders are designed to operate at a high performance mode in order to complete a maximum number of iterations within a given timing deadline.The design is strictly pessimistic since a codeblock would reach convergence with fewer iterations than the preset maximum. In order to reclaim the timing slack and slowdown the decoder in switch to low-power mode.

Fig. shows a decoding task performed in both high and lowpower mode. In high-power mode the task is completed before a timing deadline, while in low-power mode the task is also completed within deadline but utilizes the full slack that remains from the high-power mode. Each curve indicates the total energy spent for each task. Energy efficiency may be improved by reclaiming the slack left depending upon the relationship among the power levels and the slowdown factor, when running under the high power mode.

### A. Previous Work

Previous works of power management on iterative decoders focus on reducing the number of iterations to avoid unnecessary decoder operation. Iteration control techniques to detect the convergence or not of a codeblock and decide whether to halt the decoding task. This is called hard or soft decisions. Hard-decision aided (HDA) criteria are obtained as a function of binary-decision values from the decoding process; the soft-decision aided (SDA) criteria use a non-binary-decision parameter from the decoding process that is compared with threshold values. We should monitor the sign changes of the LLRs in order to detect the codeblock convergence. SDA criteria methods monitor the cross-entropy value and the mean-reliability value .

We proposed a preprocessing stage for LDPC decoding that estimates decoding effort and the system

power mode in order to have a constant decoding-time. According to us, no other work has follow online the iterative decoding process in order to make predictions about the codeblock convergence and look for opportunities to apply dynamic power management .

DPM techniques and workload prediction have been previously proposed in different contexts. For example the MPEG frame decoding time and applies dynamic voltage scaling. we target about the embedded system applications and propose a software-based power manager that profiles the workload characteristics.

Intense research, comprehensive surveys of DPM can be found. As revealed by these works, DPM has been mostly investigated in operating systems for general purpose and embedded computing. The main problem studied is to find the optimal transition times to low-power or idle modes. In this work, we target a real-time kernel for mobile computing devices that must depends upon control policies of very low complexity in order to enable DPM. We present an adaptive predictive control scheme for iterative decoders.

## B. Problem Definition

We have to consider an iterative decoder as a power manageable CMOS component governed by a power manager. The set P= $\{P_0, P_1 \ldots\ldots\ldots\ldots, P_{n-1}\}$ defines n power modes.

$$P_k = P_k^{sw} + P_k^{sc} + P_k^{leak} = E_{sw} C_L V_k^2 f_k + I_{sc} V_k + I_{leak} V_k$$

$P_k^{sw}$ is the power due to the switching between charging and discharging the load capacitance $C_L$ with switching activity factor $E_{SW}$ . $P_K^{SC}$ is the power due to a short-circuit current when both nMOS and pMOS sections of the circuit are switched. $P_K^{leak}$ is the power due to the leakage current $I_{leak}$ constitutes subthreshold plus reverse bias junction current.Each power mode $P_K$ operates at a voltage level of $V_k$ and frequency $f_k$. we assume that the first state consumes the high power, subsequent states consume each less power than the previous one. For each power mode $P_k$ its slowdown factor $\alpha_k$ where for the fastest mode $\alpha_0 = 1$. Each power mode can also be described as a fraction of the highest power mode by a factor $\beta_k$,e.g., $P_k = \beta_k P_0$ .

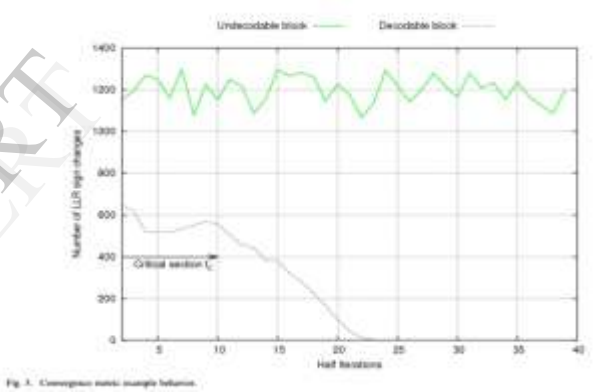
The quadratic relation between power and voltage and the linear relation between power and frequency, it is possible to slowdown the system such that the total energy consumption is reduced. This is the principle behind the well-known concept of dynamic voltage and frequency scaling (DVFS).

Given the model of the power function $P_k \alpha V_k^2$ and $f_k$ $(V_k - V_t^2)/V_k$ and due to the convexity of the power function, the power manager to run a task as slowly as possible.

The workload of iterations to be executed before a timing deadline d, to find a subset of power modes P Є R such that the total energy is minimized. If an iteration is executed within a time duration $t_k$ through a power mode $P_k$, the problem is stated as finding theoptimal $\mathcal{P}$' that minimizes the total energy spent

$$\text{minimize } \sum P_k^{(i)} t_k^{(i)}, \; P_k \in P'$$
$$\text{subject to } \sum t_k^{(i)} \leq d$$

Where $P_k^{(i)}$ indicates the power used in the i $^{th}$ iteration. This problem can be formulated as a linear program that minimizes an energy function by finding a power P Є R that guarantees the constrain d.



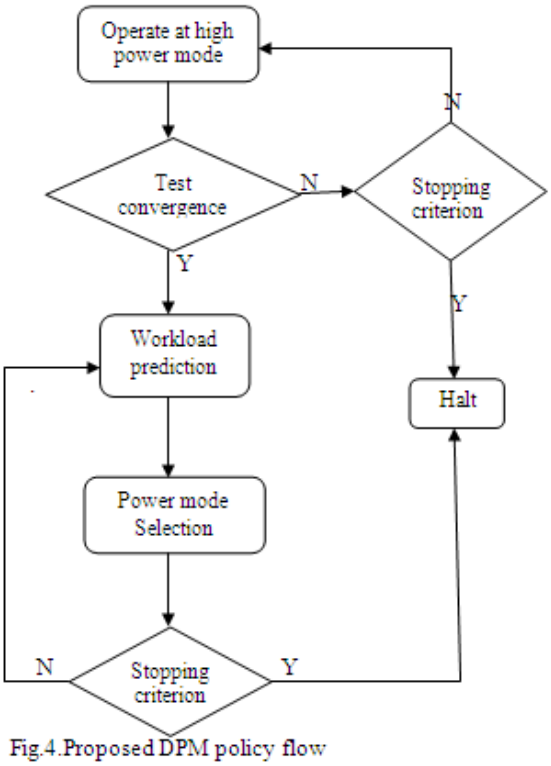



Fig.4.Proposed DPM policy flow

## C. Control Policy

DPM is at its core an online problem in which a power manager must make decisions about the system operation mode before all of the input to the system is present. The input refers to the total required number of required iterations for codeblock convergence. Instead, an online algorithm used to find an optimal power mode based upon information available only at run-time. Otherwise, an offline algorithm finds the optimal power mode assumes the total required number of decoding iterations .

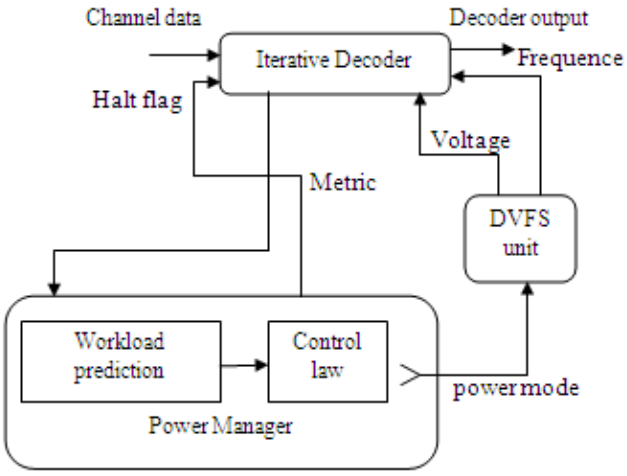



Fig.5. System block diagram

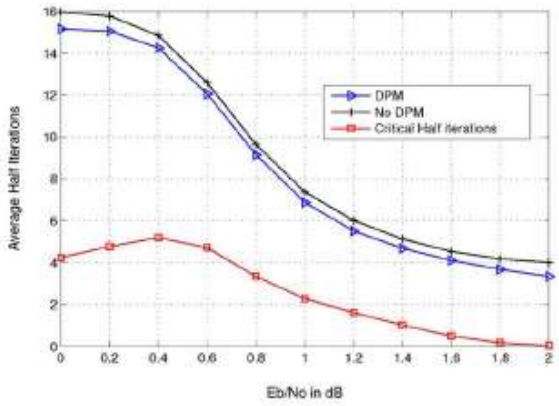
To formulate the online policy it is compulsory for the dynamics of the decoding process. We calculate to monitor the number of hard-decision changes upon the posterior messages after each half iteration, i.e., at the output of each component SISO decoder. We refer to this metric as a convergence metric and use it to make decisions (2).

Fig. 3 shows the number of sign changes in the posterior LLRs after each half-iteration for an instance of an undecodable and a decodable codeblock. The code defined in [4] with codeblock length 6144 and rate 2/3 through the additive white Gaussian channel(AWGN)( $E_b/N_0$=1 dB ) with quadrature phase shift keying (QPSK) modulation and 20 maximum full-iterations. For undecodable blocks ,the decision metric fluctuates around a mean value, but for decodable blocks it fluctuates for a period of time and later enters a convergence mode characterized by a monotonic decreasing behavior. We refer the period $t_c$ as a critical period.

As shown in Fig. 3, Due to the repeated and irregular fluctuations of the metric, no predictions can actually be valid during the critical time section. once the convergence mode is entered predictions can be made in order to approximate the probable end of the task. According to the assumption the task speed is the optimal decision in terms of energy consumption.The proposed decoder operates at a high-power mode (high speed) during the critical period and look for opportunities to slowdown (low-power modes) the system.

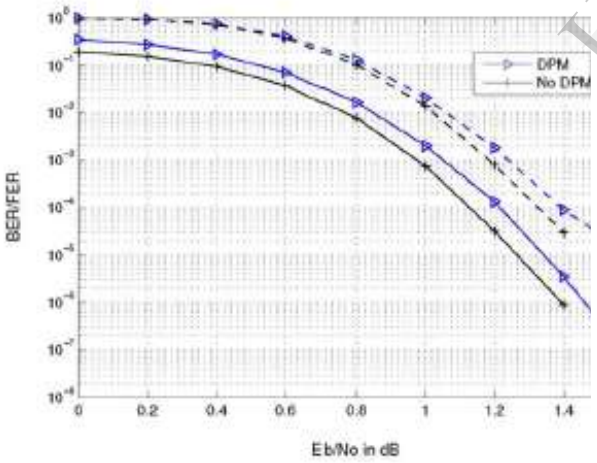
The proposed control policy based upon the observations of the selected convergence metric. Fig. 4 shows the decision flow of the control policy. Decision making is depends on the behavior of the monitored

metric that describes whether a convergence mode is entered or not and whether further decoding iterations may be triggered or not. The latter point refers to an early stopping criterion just like the ones mentioned in the previous work. In Section IV-B, explains how the performance loss in the error-correction sense based on the stopping criteria used within the power control policy. The stopping criteria suffer from false alarms.



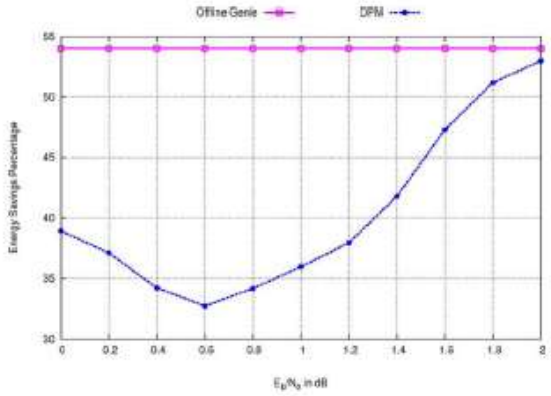

(a)

(a)Workload visualization(Result for test case K=1280 and rate 2/3 )




(b)

(b)BER/FER performance(Result for test case K=1280 and rate 2/3




(c)

(c)Average energy saving (Result for test case K=1280 and rate 2/3 )

## IV. HARDWARE IMPLEMENTATION

In this section, The proposed system for dynamic power management implements the control policy outlined in Section III-C. Results are obtained from policy simulations along with synthesized components are presented.

### A. DPM System

The proposed DPM system is shown in Fig. 5. The voltage and frequency operation of as iterative decoder is governed by a power manager. It receives intrinsic channel values in the form of LLRs and produces hard-decision bits for the message. In the decoder form power manager executes the proposed control policy by constantly monitoring a convergence metric from the decoder. The power manager sets the state of a DVFS unit that provides the operating conditions for the decoder.

The energy savings obtained from the proposed DPM policy depends upon the characteristics of the power modes used and the DVFS block implementation. There are numerous works to implement a DVFS unit, using different techniques with several tradeoffs like: size and power overhead, mode switching speed and conversion efficiency. The proposed work provides a study on on-chip regulators for DVFS implementation on a dedicated core.Both the works show sufficiently fast switching regulators (voltage transition times on the order of tens of nanoseconds) for demanding applications such as Turbo decoding.By this we get an on-chip solution to implement the DVFS unit

## B. Results

The tuning of the control policy refers to the setting of the parameters within the stopping .In conjunction with the workload characterization, refers to observations from the average number of iterations as a function of SNR. This provides insights the required workload based upon the channel quality. By observing the average number of critical iterations the stopping criterion is adjusted to limit the time the decoder will operate at a high-power mode.

The proposed DPM technique is applied to an LTE Turbo decoder uses 6 SISO radix-2 units with a window length of 32 samples with a message quantization of 6-bits, provides a throughput of 95 Mbps and completes a decoding task of 8 full iterations in 65 µs (the timing constraint value). The decoder operates on two modes: 1.2 V at 266 MHz and 0.9 V at 160 MHz. The decoder and the power manager are synthesized with Synopsys Design Compiler and the power consumption was estimated using Synopsys PrimeTime postlayout netlists along with pertinent activity files.

Due to space constraints wepresent the case of code length K = 1280 and rate 2/3. Fig. 6(a) shows the workload characterization as a function of SNR (with a max. 8 full iterations). The average of half-iterations are shown for no DPM, DPM and the average critical half-iterations. The corresponding curve to No DPM uses the stopping criterion HDA rule outlined in [8].This criterion halts the decoder once the hard -decisions upon the posterior messages change between consecutive iterations. Based upon these results and the error-correction performance loss, the DPM policy is tuned to provide the biggest gains in energy savingsat the lowest performance loss. Fig. 6(b) shows the bit-error rate (solid lines) and frame-error rate (dashed lines) (BER/FER) for applying the DPM technique.

The energy savings achieved by an offline strategy (genie) are provided to visualize how far the DPM policy behaves from its ideal performance. The offline policy produces around 54% of energy savings, this is approached by the DPM technique on the high SNR region. It comes from the fact that at high SNR values the critical workload is very low, this indicates that the blocks enter convergence relatively fast. The energy savings is acheived vary between 34% to 54% depends upon the channel quality.

TABLE I

AREA AND POWER COMPARISION

| Work | Propesed | [21](SC) | [21](PR) |
|---|---|---|---|
| Energy Savings % | 54 | 17.5 | 180 |
| SNR loss[dB] | 0.08 | 0.34 | 0.48 |

TABLE II

COMPARISION OF ENERGY SAVING TECHNIQUES

| Component | Area[$mm^2$] | Power[mW] |
|---|---|---|
| Turbo decoder (No DPM) | 0.62 | 180 |
| Power manager | 0.08 | 5 |
| DVFS unit | 0.12 | 25 |

The energy savings from the proposed policy have two components: one is due to the inherent stopping criteria and another one due to the system slowdown. The first one dominates on the low SNR region and the second on the mid to high SNR region. At low SNR the stopping criteria detect the potential codeblocks which are not likely to be decoded, whereas at the mid to high SNR values the system takes advantage of the fast convergence in order to reduce power consumption.

Revealed at Table I,the area and power overheads for applying DPM on the synthesized decoder. The DVFS unit is characterized from the results presented in [19], [20]. From that works we extract the data for a buck converter with a switching frequency of 100 MHz and a conversion efficiency in the range of 75%–87% with an output voltage range of 0.9–1.3 V

The achieved average energy savings are compared with works from the prior art in Table II. The SNR loss in the table corresponds to the point at ber = $10^{-5}$. Even though the codes among the cited works are different, the SNR loss provides a measure on the impact in performance for each applied power savings technique. The work in [21] will analyse individual techniques proposed for energy reduction in Turbo decoding. The reported achieved energy savings for reduction in the number of paths (PR) and the LLR stopping criterion (SC). By several of the analyzed techniques therein were combined and savings of up to 66% were reported.

## V. CONCLUSION

The dynamic power management policy for iterative decoders has been presented. This technique is aided by the dynamics of the decoding process which can be extracted from a particular convergence metric. Once, the decoder has entered a convergence mode,the judicious selection of a power mode is carried out during run-time by a power manager which considers the decoding task deadline and the predicted remaining decoding time. Thus the proposed technique has been applied to the decoding of Turbo codes where the total number of hard-decision changes in the posterior messages was used as a decision metric. In this the energy savings of up to 54% were achieved with a relatively low impact on error-correction performance.

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