

Test Patterns Generator for Bist Schemes using Multiple SIC Vectors on FPGA

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Abstract— To deal with the increased switching activity in SOC, this method present a new built-in self- test (BIST) scheme for low energy testing that uses a multiple single input change (MSIC) vector in a test pattern. In this method SIC vector generator could reduce the switching activity in scan cells during scan-in shifting and applied to scan chain. The goal of this technique to minimize the power consumption during test mode in BIST. The SIC vector generator uses a reconfigurable Johnson counter or scalable SIC counter are used to generate a minimum transition sequences. Based on this MSIC-TPG pattern to reduce a test power and also achieve a low hardware overhead. By using this method easy to achieve both Test-per-clock and Test-per-scan of test pattern applied to circuit under test (CUT) and implemented in VHDL. MSIC-TPG sequence should not contain any repeated test patterns and also to find the target fault coverage without raising the test length. The experimental result provided the high performance which is applied to ISCAS benchmarks circuitry. Design is verified on FPGA Spartan3E.

Key Words: Built-in self-test (BIST), low power, single-input change (SIC), test pattern generator (TPG).

I. INTRODUCTION

SOC circuits depends on testing to eliminate various defects caused by the manufacturing process. With the advance in semiconductor manufacturing technology, leads to increases in chip's complexity and volume. Many challenges are imposed on tools and methodologies used to design and test complex VLSI circuits. The most important issues in the development process of an integrated circuit during testing are manufacturing yield, product quality, and test cost. To address these test issues, Design for testability (DFT) is a methodology that improves the testability, in terms of controllability and observability, thereby making the test generation and circuit fault coverage easier.

To describe manufacturing defects and their fault models in the circuits, test patterns are generator which is applied to the circuit under test (CUT) and to detect faulty circuits can be done either externally using automatic test equipment (ATE) or internally using built-in self-test (BIST). External testing using ATE are expensive and become more and more inefficient. This makes at-speed testing extremely

difficult. BIST is fast becoming an alternative solution to ATE, which is a DFT method where parts of the circuit are used to test the circuit itself. Test vectors for BIST circuits are generated applied to the circuit-under-test and output response analysis (ORA) using on-chip circuitry, lessening hardware overhead is a major concern of BIST implementation and also reduced the difficulty in VLSI testing. There is a problem occur in BIST, if switching activity in a circuit can be significantly higher than normal operation and hardware area overhead.

II. BACKGROUND

Built-in self-test (BIST) schemes can be classified into (a) test-per-clock and (b) test-per-scan, according to the way in which test patterns are applied to the CUT. In test-per-clock BIST, test vectors are applied every clock cycle from the TPG, and test responses are captured in the ORA and compared to a reference value. This scheme has the advantage of running much faster in applying tests and yields higher fault coverage than test-per-scan BIST. The drawbacks of this scheme are high area overhead and incompatibility with scan design.

In test-per-scan BIST, also called scan-based BIST, patterns are first shifted into the scan chains during shift operation; the test responses to these patterns are then captured in scan cells during the capture operation. The captured test responses are shifted out to the ORA for response compaction while a new test is being shifted in. When a CUT has long scan chains, most switching activity in the CUT will occur during scan shifting. As a result of the excessive switching activity, power consumption will increase, thus reducing battery lifetime, and also causing heat dissipation which may permanently damage the CUT.

Several techniques [2] that have been developed to reduce the power dissipated during scan-based test. Bit-swapping LFSR technique of power reduction occur during test mode is easy to implement, significantly increases the test application time. The design of low transition RTPGs [3] is one of the common and efficient techniques for low power test. These techniques can reduce the transitions in the scan inputs by assigning the same value to most neighboring bits in the scan chain. The main drawback of these algorithms is that they may result in lower fault coverage and higher test application time since some random features are lost in the patterns generated by these techniques. Another category of

techniques smoother [5] is used at the output sequence of a LFSR, which is applied to scan-chain input of test-per-scan scheme. These can achieve different degrees of smoothed patterns depending on the selected smoothing degree and the design has a very small hardware area overhead and a negligible effect on fault coverage or test application time.

This paper presents a new approach, a Multiple Single Input Change (MSIC) vectors are used as test pattern generators for BIST circuits. MSIC sequence had the favorable features of uniform distribution, low input transition density, and low area overhead. The proposed design achieves the target fault coverage without increasing the test length and also increase the test efficiency. Hence proposed TPG is applicable to both the test-per-clock and the test-per-scan schemes.

III. OVERVIEW

In these techniques have been proposed for designing an on-chip test generators that can generate an effective test patterns while reducing the transition density in the CUT. The use of MSIC vectors converted in to SIC vector which is applied to all multiple scan chains using TPG.

Hence, a test pattern with similar test vectors will be applied to all scan chain. These SIC sequence is a low power approach which greatly decreased the transitions for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting and reduce power. The minimum transition sequence are generate in test vector using SIC sequence to develop either a reconfigurable Johnson counter or a scalable SIC counter. For short scan length, a Johnson counter is to generate an SIC sequence. If the scan chain length is maximum then we develop an SIC counter named as “scalable SIC counter”.

The MSIC-TPG of TPC structure is shown in fig. 1, this scheme has the advantage of running much faster in applying tests and yields higher fault coverage than test-per-scan BIST. The drawbacks of this scheme are high area overhead and incompatibility with scan design. To reduce the area overhead and also takes advantage of the scan design thereby reducing switching activities is a test-per-scan of MSIC-TPG structure as shown in fig.2, is a much simpler BIST circuitry.

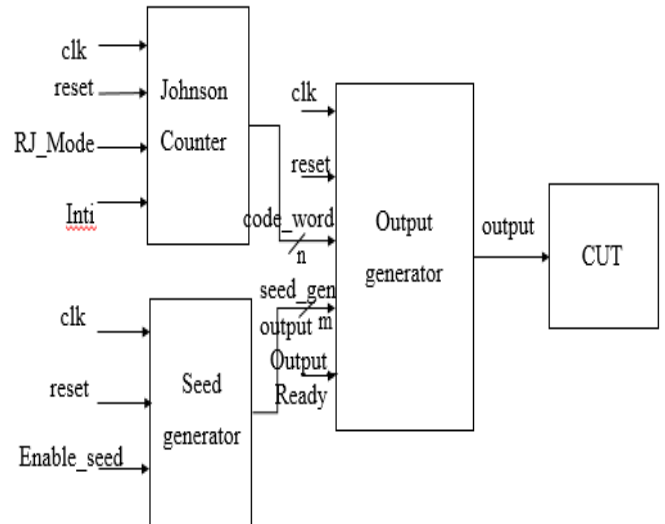


Fig.1. Test-per-clock MSIC-TPG structure

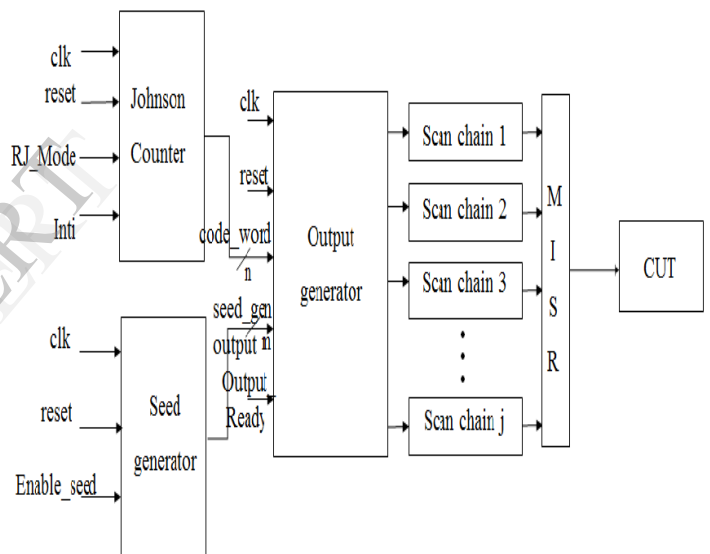


Fig.2. Test-per-scan MSIC-TPG structure

This TPC and TPS of MSIC circuits has been implemented using VHDL programming language. Xilinx 14.2 ISE simulator is used to produce RTL model for proposed BIST architecture for a given set of test algorithms. The RTL view for Test-per-Clock and Test-per-Scan as shown in fig. 3 and 4.

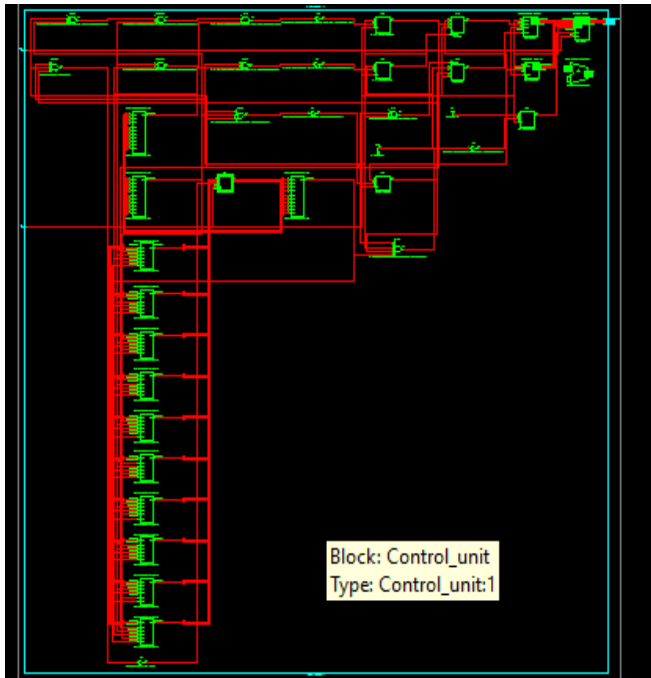


Fig. 3. RTL schematic for Test-per-Clock

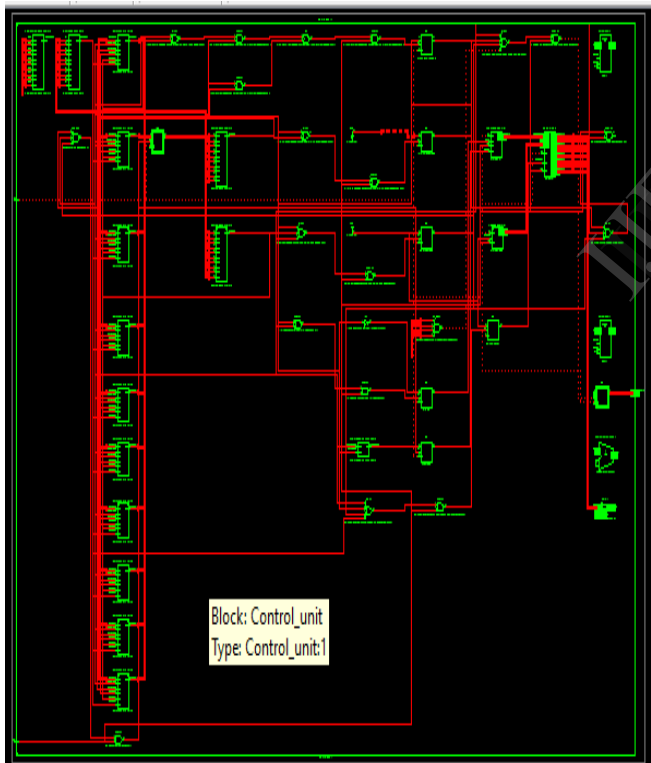


Fig.4. RTL schematic for Test-per-Scan

A. Overview of the Algorithm

The steps in the algorithm can be summarized as follows:

- 1) The seed generator generates a new seed by clocking CLK one time using enable seed.
- 2) RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK one time.

3) After a new Johnson vector is generated, RJ_Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates n codewords by clocking CLK n times. Then, a capture operation is inserted.

4) If $2n$ Johnson vectors are generated and then XOR the output of seed_generator with Johnson codeword in the output generator.

5) Output generator outputs are applied to j scan chain input and achieved the minimum transition.

6) The procedure are repeated until the expected fault coverage is achieved.

B. Construction of a Reconfigurable Johnson Counter

A Johnson counter is a modified ring counter, if inverted output of last flip flop is connected to the input of first flip flop. These register cycles which is applied to a sequence of bit-patterns. The fig.5, shows that the reconfigurable Johnson counter, it consists of AND gate, mux, and n number of D flip flop is used. If n represents the maximum scan chain number.

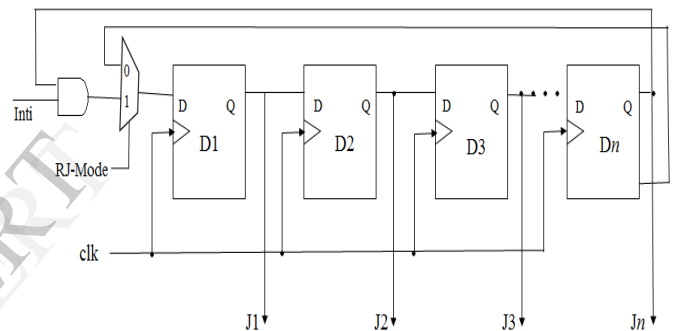


Fig. 5. Reconfigurable Johnson counter structure

Johnson counter can operate in three modes of operation.

1) Initialization

When RJ_Mode is set to logic 1 and Init is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK more than n times.

2) Circular shift register mode

When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will produced output of Johnson codeword by clocking CLK n times.

3) Normal mode

When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate $2n$ unique SIC vectors by clocking CLK $2n$ times and new Johnson vector applied to XOR gate.

Thus to implement a Johnson counter in to MSIC-TPG scheme the overhead can effectively decreased and to reduce area. For these purpose this counter which is used in scan design.

C. SIC Vectors

By using a SIC vectors to achieve the minimum transition and applied to multiple scan chains as shown in

figure 6 representation of MSIC pattern that consists of the vector that are generated by an n-bit Johnson counter can be expressed as $J(t) = J_0(t) J_1(t) J_2(t), \dots, J_{n-1}(t)$. The SIC vectors is developed to set RJ_Mode as logic 0, then reconfigurable Johnson counter will generate a $2n$ unique SIC vectors by clocking CLK $2n$ times, so the SIC vector is decompressed to its multiple Codewords and then generated codewords will bit-XOR with a seed vector called as output generator. The vector that are generated by an m-bit seed generator can be expressed as $S(t) = S_0(t) S_1(t) S_2(t), \dots, S_{m-1}(t)$. So this output generator has consists of codewords and seed generator are applied to multiple scan chain to reduce the transition. A full scan design consists of m primary inputs (PIs) and j scan chains and each scan chain has n scan cells. A Compression schemes is based on using linear decompressors to expand the data coming from the tester to fill the scan chains during test application.

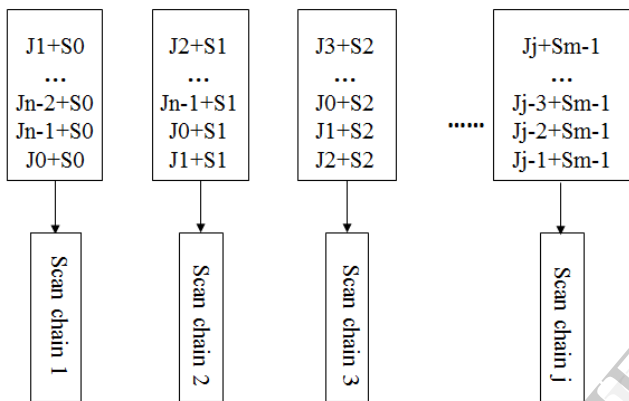


Fig.6. Symbolic representation of an MSIC pattern

In the MSIC pattern, each generated vector applied to each scan chain is an SIC vector, which can minimize the input transition and reduce test power. Hence uniqueness of pattern is also achieved, these sequence does not contain any repeated patterns, and also meet the requirement of the target fault coverage for the CUT. Hence, the MSIC TPG can be easily implemented by hardware.

IV. HARDWARE IMPLEMENTATION

The proposed TPG based BIST are programmed on VHDL language and are implemented on FPGA Spartan3E. Thus, the proposed scheme greatly simplifies the testing process. Besides, the proposed is more efficient in terms of circuit size and test data to be applied, and it requires less time to configure the BIST. Thus Xilinx 14.2 ISE simulator is used to produce RTL schematic view for proposed BIST architecture. After synthesis and implementation, we can use the XPower Analyzer to get a detailed view of the power distribution for design. This allows to determine whether the design meets power requirements. For designs that do not meet power requirements, the XPower Analyzer assists in finding ways to minimize dynamic power, such as using power reduction techniques or modifying software options. Toggle rate of proposed BIST is 12.5%.

V. RESULT

The correctness of operation was verified using ModelSim simulator. The verification tool is used to simulate and verify the output of the design. It produces the waveform from which the behavior of the design can be analyzed and the waveform for test-per-clock and test-per-scan are displayed in fig. 7 and fig. 8. The number of flip flops and logic gates that are used for TPC are 74 and 139. In TPS 8 scan chain is used here and each scan chain has 8 scan cell. The number of flip flops used for TPS is 152 and the LUT that are used for this is 49%. Hence device utilization summery as shown in the fig. 9.

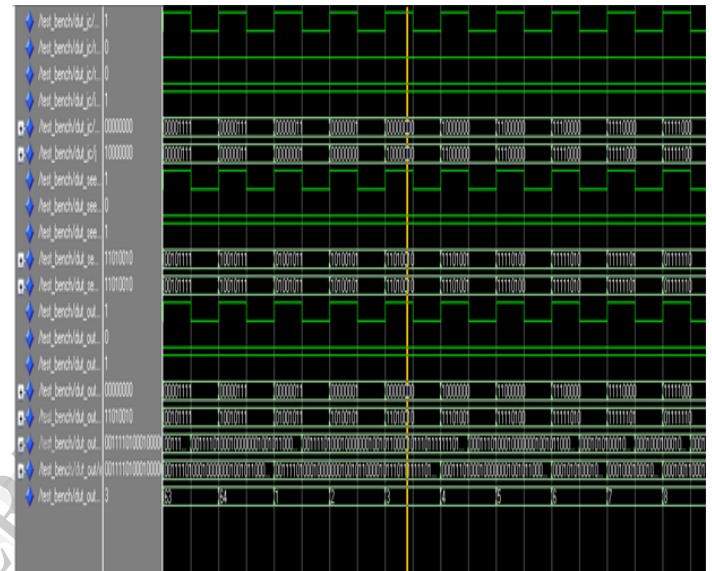


Fig. 7. Waveform for Test-per-Clock

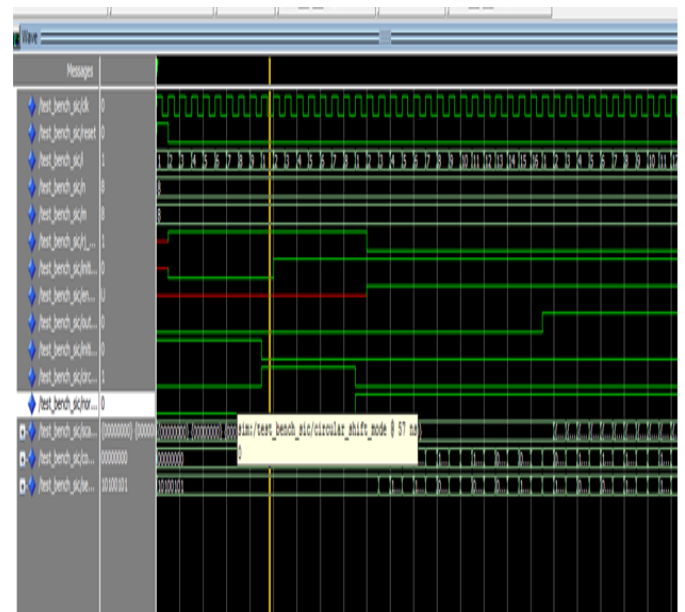


Fig.8. Waveform for Test-per-scan

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	152	9,312	1%
Number of 4 input LUTs	2,640	9,312	28%
Number of occupied Slices	2,359	4,656	50%
Number of Slices containing only related logic	2,359	2,359	100%
Number of Slices containing unrelated logic	0	2,359	0%
Total Number of 4 input LUTs	4,579	9,312	49%

Fig.9. Synthesis Result

The result of compilation of Xpower analyzer analyze the power dissipation is furnished below

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device		On-Chip	Power (W)	Used	Available	Utilization (%)				Supply Summary	Total	Dynamic	Quiescent
Family	Spartan3e	Clocks	0.000	1	--	--				Source	Voltage	Current (A)	Current (A)
Part	xc3s500e	Logic	0.000	4571	9312	49				Vccint	1.200	0.026	0.000
Package	fg320	Signals	0.000	4964	--	--				Vccaux	2.500	0.018	0.000
Temp Grade	Commercial	IOe	0.000	10	232	4				Vcc025	2.500	0.002	0.000
Process	Typical	Leakage	0.081										
Speed Grade	-5	Total	0.081										
Environment		Effective TjA	Max Ambient	Junction Temp									
Ambient Temp (C)	25.0	Thermal Properties	(C/W)	(C)	(C)								
Use custom TjA?	No		26.1	82.9	27.1								
Custom TjA (C/W)	NA												
Airflow (LFM)	0												
Characterization													
PRODUCTION	v1.2.06-23-09												

Fig.10. Power analysis

Experiments were performed on standard ISCAS-89 benchmark circuits: s1512, s5378, s15850. For each circuits we used to simulate using ModelSim simulator as displayed in fig.11. The number of scan chain used for s1512 is 29 and each scan chain has 29 scan cell. The scan chain used for s5378 is 35 and each scan chain has 35 scan cell. In s15850 used 77 number of scan chain and each has 77 scan cell. Hence power reduction has been obtained.

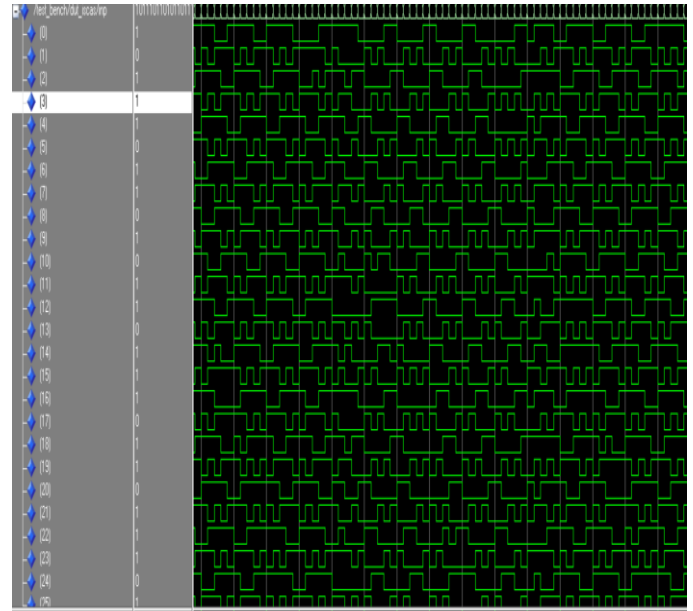


Fig.11. waveform for s1512

TABLE I. RESULT SHOWING POWER REDUCTION AND AREA OVERHEAD

Parameter	Test-per-clock	Test-per-scan
Registers	74	152
Number of LUT in %	1	49
Frequency in MHZ	168.628	2.678
Power in mW	81.18	69.79
Total Memory usage in Kbytes	263596	254188

VI. CONCLUSIONS

In this method a new low power MSIC-TPG test patterns is achieved during test mode. The switching activity in the CUT are also reduced by using SIC sequence of reconfigurable Johnson counter or scalable SIC counter is implemented in both Test-per-clock and Test-per-scan testing. The MSIC sequence should not contain any repeated test patterns. So thus the proposed system improves the test efficiency and reduced the test time. Experimental results showed that the area overhead can be controlled under reasonable range. Thus the satisfied fault coverage is also achieved without increase the test length.

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