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The Influence of Physical and Geometrical Parameters on the Electrical Characteristics of Gan MESFET

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***Abstract*—in this study we used the simulator TCAD-SILVACO (ATLAS) for the simulation of the electrical behavior of GaN MESFET. The main types of characterizations intended that the drain current is expressed as a function of gate voltage or drain. Note mainly IDS (VDS), IDS (VGS) characteristics.**

A clear study of the various parameters used by the simulation provided a better understanding of the causes generating the drain current by studying the influence of different parameters: doping of the active layer, the thickness of the active layer, channel length and length of gate Lg on the characteristics Ids (Vds).

Keywords— GaN; MESFET; ATLAS simulator; Drain current; Saturation velocity; doping; gate length; channel.

I. INTRODUCTION

The GaN MESFET usually includes an active layer of n-type semiconductor formed on a insulating substrate, two ohmic contact (source and drain) and a metallic gate deposited halfway between drain and source in terms of creating a Schottky barrier .

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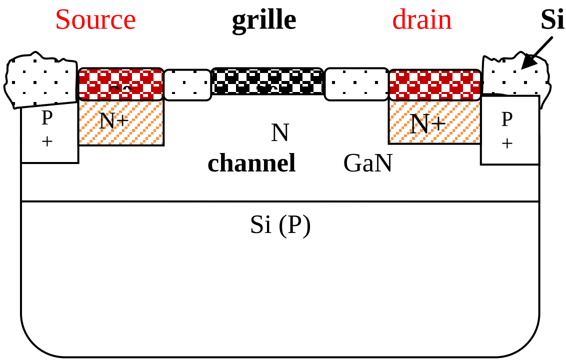

Fig. 1. structure d'un MESFET GaN

The active layer is epitaxially deposited on the insulating semiconductor substrate. It is then etched to obtain a block in which the transistor is made. The ohmic contacts of the source and drain are obtained by alloying.

The active layer is directly implanted in the insulating semiconductor substrate. The refractory metal gate is then deposited. Two N + regions are then implanted in two self aligned to the gate of access zones.

The MESFET has its excellent performance in three key properties [1]:

- The presence of semi insulating substrate against which the pinch channel.
- The ability to use a control electrode of the Schottky type.
- The high electron mobility of GaN.

II. CALCULATION OF DRAIN CURRENT ID

A. *Méthode 1 résistance variable*

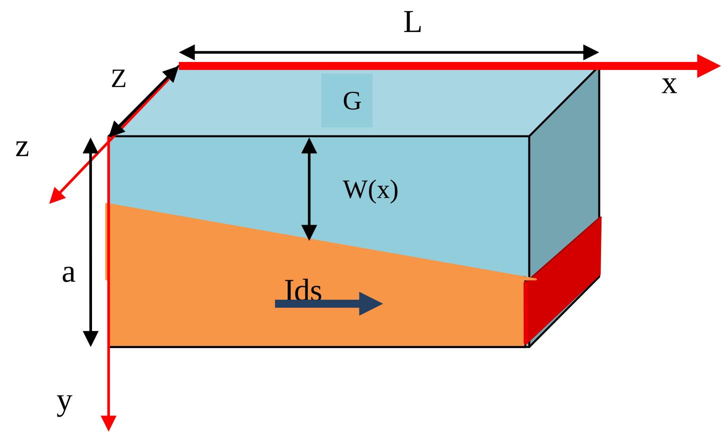

Fig2 : operating principle of GaN MESFET

If a very small current flows under the grid (very low Vds) La resistance R under the gate.

$$R = \frac{1}{\sigma}\frac{L}{(a-w)Z} \qquad (1)$$

Où σ=conductivity of the active layer
Width of the Schottky contact ZCE:

$$W = \sqrt{\frac{2\varepsilon sc}{qND}(\psi - VG)} \qquad (2)$$

$\sigma = q\mu n\ ND$ (3)

Ψ: Diffusion potential

$\psi = \phi_M - \phi_S$

ϕ_M: Work function metal

Φ_S : Work function semiconductor

$$R(V_G) = \frac{1}{q\mu_n N_D} \cdot \frac{L}{\left(a - \sqrt{\frac{2\varepsilon_{sc}}{qN_D}(\psi - V_G)}\right)Z} \qquad (4)$$

$$dR = \frac{1}{\sigma}\frac{dy}{(a - w(x))Z} \qquad (5)$$

$$w(x) = \sqrt{\frac{2\varepsilon_{sc}}{qN_D}(\psi - V_G)}$$

$V_G = V_{GS} - V(x)$ (6)

$$dV = I_D dR$$

If we integrate over the channel length L:

$$\int_{V_S=0}^{V_d=V_{ds}} \left[a - \left(\sqrt{\frac{2\varepsilon_{sc}}{qN_D}(\psi + V(x) - V_{GS})}\right)\right] dV = \int_0^L \frac{I_D\, dx}{q\mu_n N_D Z} \qquad (7)$$

$$\left[aV(x) - \frac{2}{3}(\frac{2\varepsilon_{SC}}{qN_D}(\psi + V(x) - V_{GS})^{3/2}\right]_0^{V_{ds}} = \frac{I_D}{q\mu_n N_D Z}[x]_0^L \qquad (8)$$

Are obtained:

$$I_D = \frac{q\mu_n N_D Za}{L} \times \left[V_{ds} - \frac{2}{3}\sqrt{\frac{2\varepsilon_{SC}}{qN_D a^2}}\left((\psi + V_{ds} - V_{GS})^{3/2} - (\psi - V_{GS})^{3/2}\right)\right] \qquad (9)$$

For the low Vds << [Vd -Vgs]

A Limited development is carried out by considering:

$$(1 + x)^n = 1 + \frac{nx}{1!} + \frac{n(n-1)x^2}{2!} + \cdots$$

Writing:

$$I_D = G_0\left[V_{ds} - \frac{2}{3}\frac{1}{\sqrt{V_p}}(\psi - V_{GS})^{3/2}\left(\left(1 - \frac{V_{ds}}{\psi - V_{GS}}\right)^{3/2} - 1\right)\right] \qquad (10)$$

Are obtained:

$$I_D = G_0[1 - \sqrt{\frac{\psi - V_{GS}}{V_p}}]V_{ds}] \qquad (11)$$

G0: the channel conductance.

B. Method 2: gate channel potential:

The depletion region W_n is given by the depletion width for a diode. Where the voltage is the voltage from the gate to the channel, where the channel voltage is given for a position x along the channel as $V_{gc}(x)$.

$$W(x) = \sqrt{\frac{2\varepsilon_0\varepsilon_r(\psi - V_{gc}(x))}{qN_d}} \qquad (12)$$

$$W(x)^2 = \frac{2\varepsilon_0\varepsilon_r(\psi - V_{gc}(x))}{qN_d} \qquad (13)$$

$$\frac{W(x)^2 .\, qN_d}{2\varepsilon_0\varepsilon_r} = \psi - V_{gc}(x) \qquad (14)$$

$$V_{gc}(x) = \psi - \frac{W(x)^2 .\, qN_d}{2\varepsilon_0\varepsilon_r} \qquad (15)$$

$$\frac{dV_{gc}(x)}{dW(x)} = -\frac{2W(x) .qN_d}{2\varepsilon_0\varepsilon_r} \qquad (16)$$

The current density in the channel is given by:

$J = \sigma E$ (17)

$I(x) = \sigma E . Z . b(x)$ (18)

$$I(x) = -\sigma\frac{dV_{gc}(x)}{dx} Z(a - W(x)) \qquad (19)$$

$$E = -\frac{dV_{gc}(x)}{dx} \qquad (20)$$

$$I(x) = -\sigma aZ\left(1 - \frac{W(x)}{a}\right)\frac{dV_{gc}(x)}{dW(x)}\frac{dW(x)}{dx} \qquad (21)$$

$$\int_0^L I(x)\,dx = \int_0^L -\sigma aZ\left(1 - \frac{W(x)}{a}\right)\frac{dV_{gc}(x)}{dW(x)}\frac{dW(x)}{dx}\,dx \qquad (22)$$

$$I.L = -\sigma aZ\int_{W(0)}^{W(L)}\left(1 - \frac{W(x)}{a}\right)\frac{dV_{gc}(x)}{dW(x)}\, dW(x) \qquad (23)$$

$$I = \frac{-\sigma aZ}{L}\int_{W(0)}^{W(L)}\left(1 - \frac{W(x)}{a}\right)\left(-\frac{2W(x) .qN_d}{2\varepsilon_0\varepsilon_r}\right) dW(x) \qquad (24)$$

$$I = \frac{\sigma aZ2qN_d}{2\varepsilon_0\varepsilon_r L}\int_{W(0)}^{W(L)}\left(W(x) - \frac{W(x)^2}{a}\right) dW(x) \qquad (25)$$

$$I = \frac{2\sigma aZqN_d}{2\varepsilon_0\varepsilon_r L})\left[\frac{W(x)^2}{2} - \frac{W(x)^3}{3a}\right]_{W(0)}^{W(L)} \qquad (26)$$

$$I = \frac{2\sigma aZa^2}{6\varepsilon_0\varepsilon_r L}\left[\frac{3(W(L)^2 - W(0)^2)}{a^2} - \frac{2(W(L)^3 - W(0)^3)}{a^3}\right] \qquad (27)$$

The threshold voltage of a MESFET Vt0 is the voltage required to fully deplete the channel layer. This threshold voltage is equal to

$$V_p = \psi - V_{t0} = \frac{qN_d a^2}{2\varepsilon_0\varepsilon_r L} \qquad (28)$$

$$\beta = \frac{\sigma a}{3LV_p} \qquad (29)$$

β est la conductance du canal

d is the ratio of channel depletion to maximum depletion for the drain.

S is *the* ratio of channel depletion to maximum depletion for the source..

$$d=\frac{W_n(L)}{a}=\frac{\sqrt{\frac{2\varepsilon_0\varepsilon_r(\psi-V_{gd})}{qN_d}}}{\sqrt{\frac{2\varepsilon_0\varepsilon_r(\psi-V_{t0})}{qN_d}}}=\sqrt{\frac{\psi-V_{gd}}{V_p}} \qquad (30)$$

$$s=\frac{W_n(0)}{a}=\frac{\sqrt{\frac{2\varepsilon_0\varepsilon_r(\psi-V_{gs})}{qN_d}}}{\sqrt{\frac{2\varepsilon_0\varepsilon_r(\psi-V_{t0})}{qN_d}}}=\sqrt{\frac{\psi-V_{gs}}{V_p}} \qquad (31)$$

Substitution:

$$I_n = W\frac{\sigma a.V_p}{3L}[3(d^2-s^2)-3(d^3-s^3)] \qquad (32)$$

$$I_n = W.\beta[3(d^2-s^2)-3(d^3-s^3)] \qquad (33)$$

When the transistor switches to the saturation state, one end of which pinched (typically the drain).Thus, d = 1 and we can derive the equation of the saturation region:

$$I_{sat}=W.\beta {V_p}^2[1-3s^2+2s^3] \qquad (34)$$

Le simple model est

$$I_{ds}=\frac{3}{2}\beta {V_p}^2\left[\frac{(V_{gs}-V_{t0})^2}{V_P^2}-\frac{(V_{gd}-V_{t0})^2}{V_P^2}\right] \qquad (35)$$

C. New model [4]

One of the first large signal models was proposed by Van Tuyl and Liechti. It was then refined by Curtice, which became the basis for many models. Curtice modeled transition of the linear region to the saturation with a hyperbolic function TAN [5].

$$\boldsymbol{I_{ds}(V_{gs,}V_{ds})=\beta(V_{gs}-V_{t0})^2(1+\lambda V_{ds})\tanh(\alpha V_{ds})} \qquad (36)$$

The current can be approximately calculated by assuming that all carriers at the channel opening are moving at their saturated velocity. For a constant channel doping, the saturated drain current I DS should then vary as:

$$\boldsymbol{I_{dsat}=Wv_{sat}\sqrt{2\varepsilon qN_d}\left(\sqrt{(-V_t+V_b)}-\sqrt{(-V_{gs}+V_b)}\right)} \qquad (37)$$

Each junction capacitance has been represented as a function of its junction capacitance at thermal equilibrium gate junction capacitance (Cjo), junction voltage (V), built in junction voltage (Vb) and capacitance gradient factor (m). The capacitance can be expressed as:

$$\mathbf{C}=\frac{\mathbf{C_{j0}}}{\left(\mathbf{1}-\frac{\mathbf{V}}{\mathbf{Vb}}\right)^{\mathbf{m}}} \qquad (38)$$

$$\mathrm{og}(\mathrm{C_{j0}}/\mathrm{C})=\mathrm{mlog}(\mathrm{V})-\mathrm{mlog}(\mathrm{Vb}) \qquad (39)$$

The charge under the gate Qg given by the following expression

For Vds >> 0

$$Q_g=C_{gs0}.V_b\left(1-\sqrt{1-\frac{V_{gs}}{V_b}}\right)+C_{gd0}.V_{gd} \qquad (40)$$

For Vds<<0

$$Q_g=C_{gs0}.V_b\left(1-\sqrt{1-\frac{V_{gs}}{V_b}}\right)+C_{gd0}.V_{gs} \qquad (41)$$

We can write:

$$Q=2C_{gs0}.V_b\left(1-\sqrt{1-\frac{V_{eff1}}{V_b}}\right)+C_{gd0}.V_{eff2} \qquad (42)$$

The terminology (-V_{eff1}) is meant to stand for the smaller of the two values of (-V_{gd}) or (-V_{gs}) and (-V_{eff2}) for the larger of the two.

$$V_{eff1}=\frac{1}{2}\left\{V_{gs}+V_{gd}+\sqrt{(V_{gs}-V_{gd})^2+\Delta^2}\right\} \qquad (43)$$

$$V_{eff2}=\frac{1}{2}\left\{V_{gs}+V_{gd}+\sqrt{(V_{gs}-V_{gd})^2+\Delta^2}\right\} \qquad (44)$$

Δ = 1 / α = capacitance transition width (dc parameter width (V.)

Another expression of Qg.

$$Q_g=C_{gs0}\left\{2.V_b\left(1-\sqrt{1-\frac{V_{max}}{V_b}}\right)+\frac{V_{eff1}-V_{max}}{\sqrt{1-\frac{V_{max}}{V_b}}}\right\}+C_{gd0}.V_{eff2} \qquad (45)$$

The model of statz is :

$$V_{new}=\frac{1}{2}\left(V_{eff1}+V_t+\sqrt{\Delta^2+(V_{eff1}-V_t)^2}\right) \qquad (46)$$

Cgs and Cgd are given by (see Appendix)

III. RESULTS AND DISCUSSION

ATLAS simulator that we have just described allows its flexibility many applications.

For example, it can serve to highlight the influence of the doping profile on the electrical properties of GaN MESFET.

The GaN MESFET models used for ATLAS stimulation have the following characteristics:

TABLE I. GAN MESFET MODELS

MESFET	***Gate length Lg***	***The thickness of silicon substrate***	***The thickness of the GaN layer***	***Doping ohmic contacts***	***The gate metal is Nickel***
model 1	0.3µm	0.5µm p doped; $10^{14}cm^{-}$	0.35µm N doped; $10^{16}cm^{-3}$	$5.10^{18}cm^{-3}$	5.1 eV
model 2	0.3µm	0.5µm dopé (p) ; $10^{12}cm$	0.35µm Dopée N ; $10^{16}cm^{-3}$	$5.10^{17}cm^{-3}$	5.1 eV
model 3	0.3µm	0.68µm dopé (p) ; $10^{12}cm$	0.22µm Dopée N ; $10^{16}cm^{-3}$	$5.10^{17}cm^{-3}$	5.1 eV

A. *Electrical characteristics IDS (VDS) of a MESFET (Model 1):*

In normal operating regime the drain is positively biased relative to the source, while the gate is negatively biased, always compared to the source.

The observation of the characteristics used to distinguish two zones of operation of field effect transistor. A region called ohmic zone in which the drain current varies linearly as a function of the voltage VDS. A second region called saturated operating region where the drain current hardly depends on the voltage VGS.

A fixed gate voltage, the increase of the positive drain voltage creates an electric field in the channel. This field causes the electrons from the source to the gate, thereby establishing a current IDS (drain - source).

We have shown in Figure 3 the characteristics Ids (Vds) for GaN MESFET for Vg = 0V.

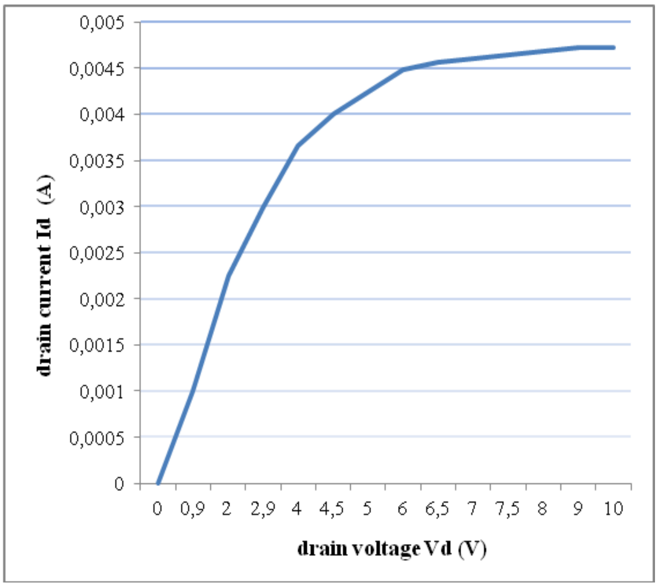

Fig3: Electrical characteristics IDS (VDS) of a MESFET (Model 1)

We note increase of the drain current when the drain voltage increases, this increase is due to the fact that the electric field intensity E increases in the active layer (channel) between the drain and the source, on the other hand the increase the electrical conductivity σ of the sum of two terms corresponding to the contribution of the electrons and holes [1].

$$\sigma = \frac{1}{\rho} = ne\mu_n + pe\mu_p \qquad (47)$$

$$\mu_n = q\tau_n/m_n \qquad (48)$$

$$\mu_p = q\tau_p/m_p \qquad (49)$$

Où $\mu_n = 1500\ cm^2/Vs$ et $\mu_p = 30\ cm^2/Vs$ the mobility of electrons and holes.

The electron velocity is given by the equation $v = \mu_n E$, we see that there is no net current saturation is why meset GaN is intended for high frequency applications

$$f_T = \frac{v_{sat}}{L_G} \qquad (50)$$

L_G is the gate length.

the width of the depleted region is directly dependent on the gate voltage applied, since VG = 0, therefore the width of the space charge region is zero, the electrons move freely in the active layer doped N.

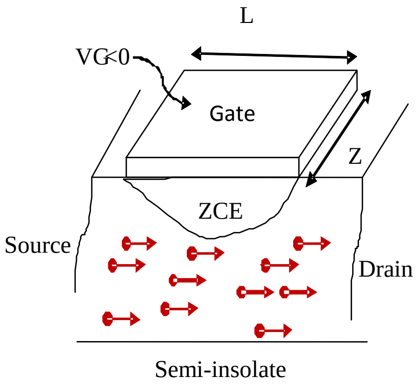

Fig4: carrier transport in the channel MESFET

B. *Characteristic $I_{DS}(V_{GS})$ for a MESFET-model 2-:*

We have shown in figure 5 the output characteristics of a MESFET (modèle 2) giving the evolution of the current Ids flowing between the drain and source when we increased the voltage Vds maintaining voltage Vgs at constant values (0, -1, -2, -3, -7, -8 and-9.5V).

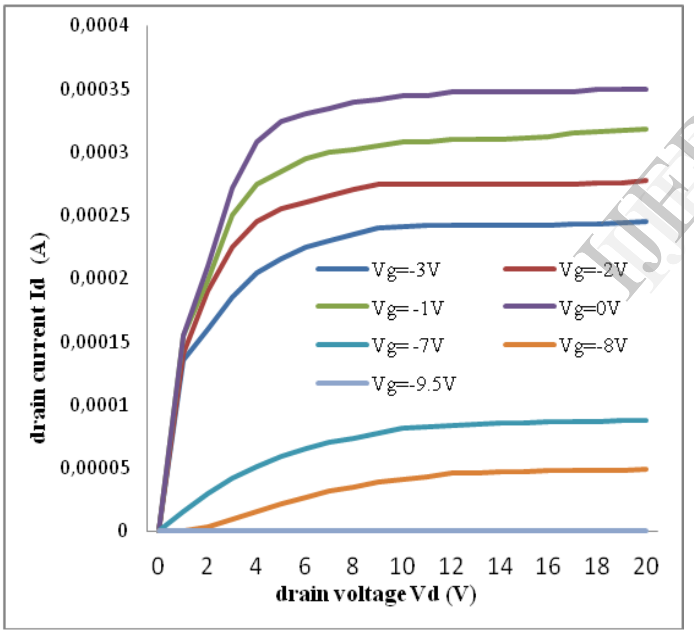

Fig5: Electrical characteristics IDS (VDS) for different values of gate voltage Vg (model 2)

For a reverse gate bias there is a decrease of drain current values reflecting the expanding space charge region in the active layer. Therefore the channel is a semiconductor layer between an insulating substrate and the space charge region of a reverse biased junction [1].

Three modes of operation can be distinguished:

- Linear regime (the current Ids increases with Vds voltage): If Vds << Vdsat.
- Saturated regime (Ids independent of Vds): If Vds >> Vdsat.
- Non-linear regime: intermediate zone between the two systems mentioned above.

The transistor switches to the saturation state when the speed of the electrons reaches their saturation velocity. For a gate voltage Vgs sufficiently negative, the channel is pinched. This threshold voltage is defined as a pinch-off voltage. [5]

C. *Characteristic IDS (VGS) for a MESFET-model 2-:*

We have shown in Figure 16 the simulated transfer characteristics is to plot the evolution of the drain-source current Ids as a function of gate-source voltage Vgs for a drain-source voltage Vds (1V and 3V).

The transfer characteristic is defined by two parameters:

☐The threshold voltage VTH, which defines the gate voltage required to pinch the channel.

☐The transconductance Gm, which defines the transfer gain: dIds / dVgs a given Vds.

$$g_m = \left.\frac{\Delta I_{ds}}{\Delta V_{gs}}\right|_{Vds=cste} \qquad (51)$$

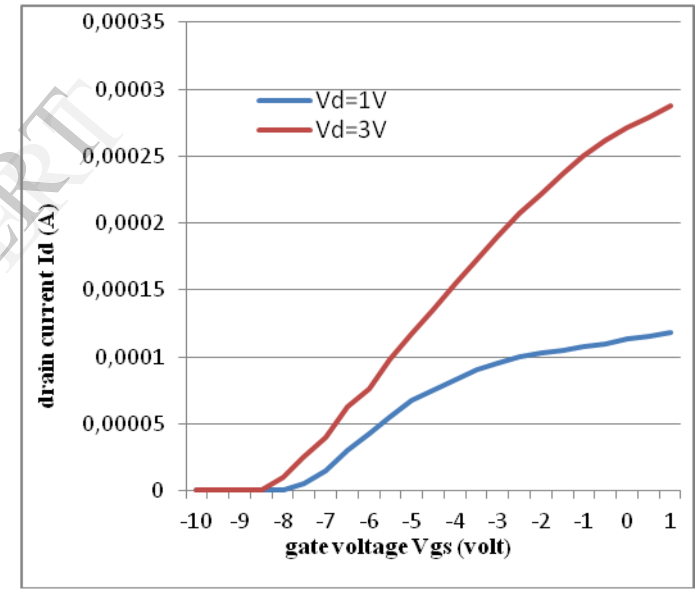

Fig6: Electrical characteristic Ids (Vgs) (model 2)

These values are shown in Figure 7 which illustrates a transfer characteristic.

The threshold voltage, VTH, is applied to the potential on the gate to empty the potential well by an elevation of the conduction band relative to the Fermi Level

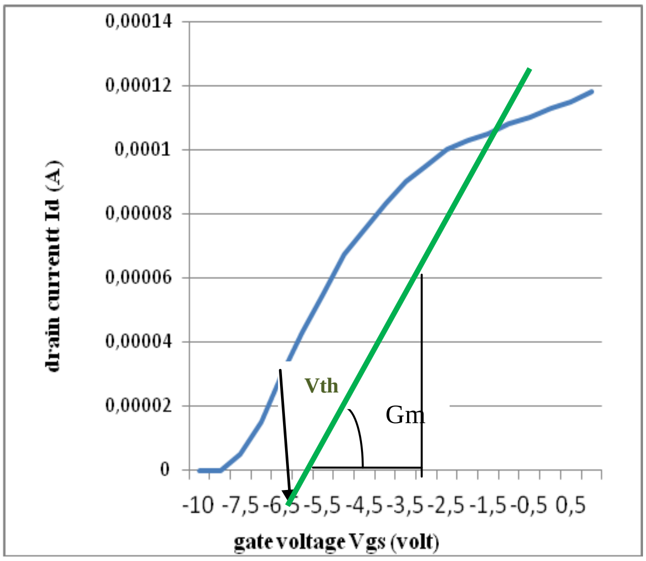

Fig7: Electrical characteristic Ids (Vgs) (model 2)

D. *Doping effect on the characteristic IDS (VDS):*

We present respectively in Figure 8 the evolution of drain current Ids (Vds) according to doping of the active layer for GaN MESFET (model2). We varied the doping of the second layer of GaN.

We note that the current IDS increases as the doping increases, so when the resistivity decreases. An increase in the doping of donor type in the GaN layer must cause a decrease in the conduction band and therefore an increase in electron density in the quantum well.

The first obvious conclusion is that we should choose a semiconductor low resistivity if we want to achieve a medium power transistor and semiconductor resistivity very high if we want to achieve a high power transistor.[6]

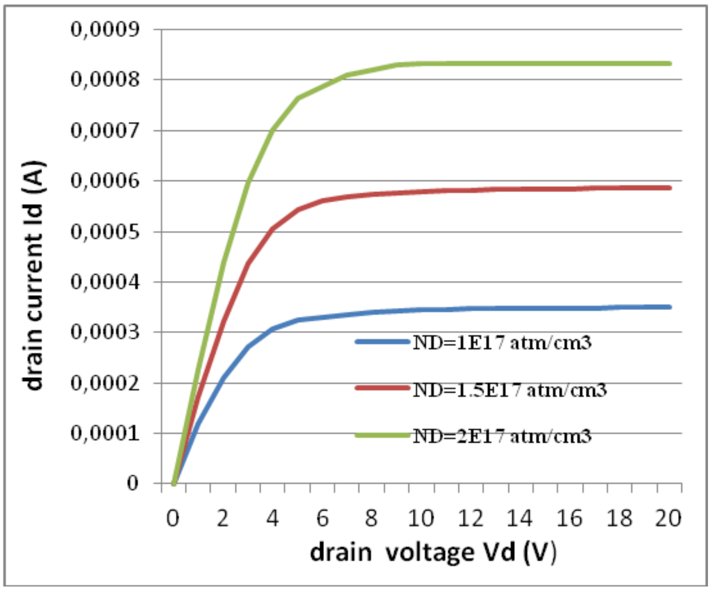

Fig8: Electrical characteristics Ids (Vds) of a MESFET (model 2) for different doping of the active layer and for ohmic contacts doping $5.10^{17}cm^{-3}$.

The variation of the drain current Ids (Vgs) for different doping of the active layer is illustrated in Figure 9, in this case the threshold voltage is reduced when Nd doping increases.

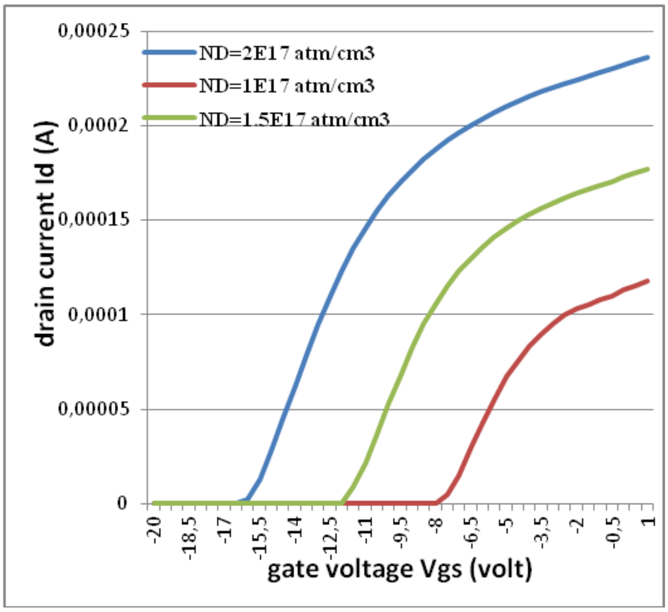

Fig9: Electrical characteristics Ids (Vgs) of a MESFET (model 2) for different doping of the active layer and the ohmic contacts a doping $5.10^{17}cm^{-3}$.

E. *Effet de la géométrie du canal :*

1) *Fine channel:*

Generally in MESFETs, a decrease in the thickness of the active layer causes an increase in the transconductance. This value reflects the resistance of the channel.

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{Vgs=cste}$$

(52)

In the case of our structure MESFET, a decrease in the thickness of the active layer causes a decrease in length of the ohmic contacts (source and drain), and thus a decrease in the drain current Ids

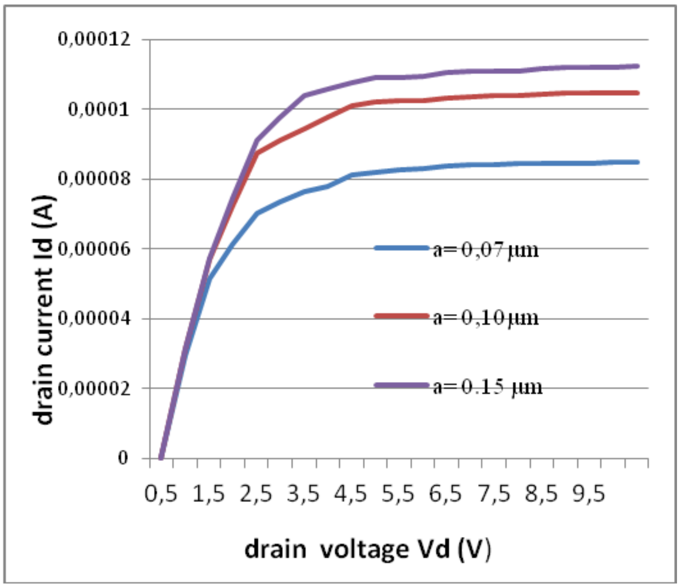

Fig10: Electrical characteristics Ids (Vds) of a MESFET (model 3) for different thicknesses of the active layer a

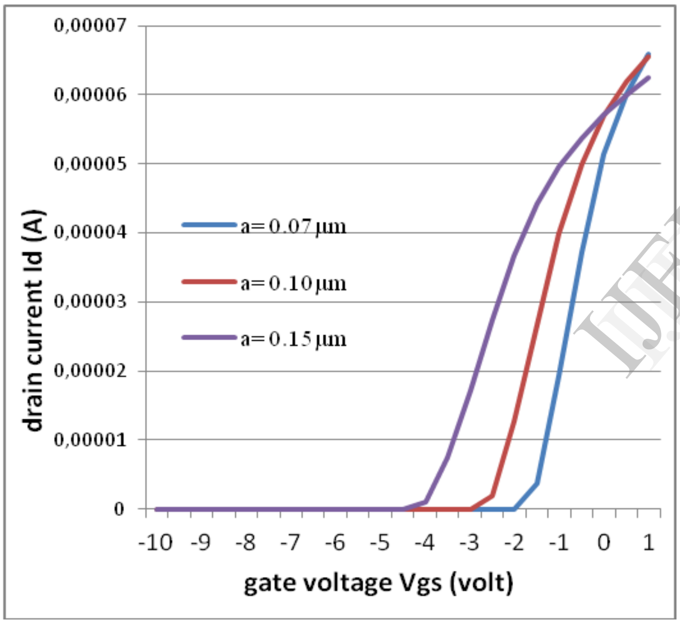

Fig11: Electrical characteristics Ids (Vgs) of a MESFET (model 3) for different thicknesses of the active layer a

2) Canal courte :

Model 4 of MESFET used for the ATLAS simulation has the following characteristics:

- The gate length Lg = 0.3µm;
- The thickness of silicon substrate Si [p-doped; 10^{12}cm^{-3}] is 0.50µm.
- The thickness of the first GaN layer [N-doped; 10^{16}cm^{-3}] is 0.35µm.
- The thickness of the second GaN layer [N-doped; 10^{17}cm^{-3}is 0.15µm.
- doping ohmic contacts is 5. 10^{17}cm^{-3}.
- The gate metal is Nickel with a work function of 5.1eV.
- Distance between the drain and the source is 1.3 µm.

The Figure 12 represents the variation of the drain current as a function of drain voltage for MESFET (model 4). It can be seen in particular that the drain current saturates; this is due to the fact that the channel length is short, which allows the electric field to reach substantial values quickly, and therefore, the rapid saturation of the carrier velocity in the channel

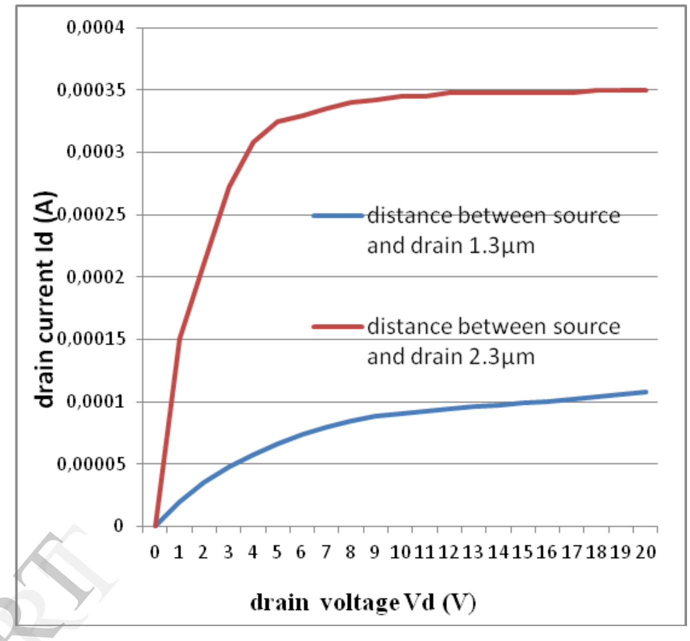

Fig12: Electrical Characteristic Ids (Vds) of a MESFET, Comparison between model 2 and 4

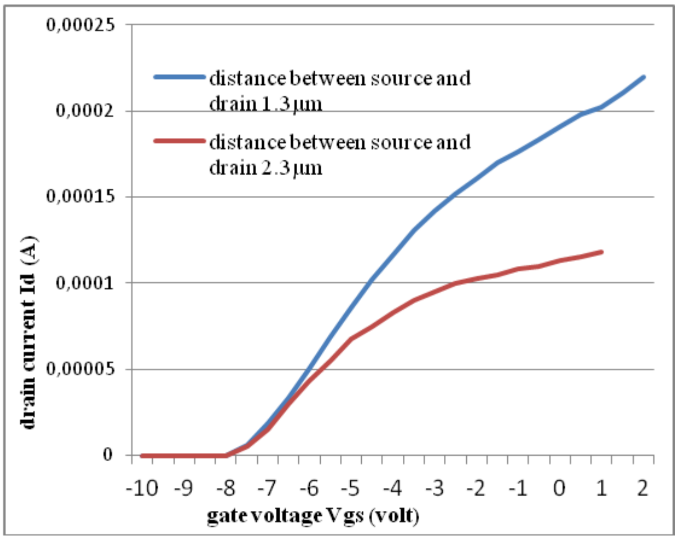

Fig13: Electrical Characteristics Ids (Vgs) of a MESFET, Comparison between model 2 and 4

3) Grille long :

Figure14 represents the variation of the drain current as a function of the drain voltage to a gate length Lg = 1.5µm, Lg = 1.1µm and Lg = 0.3µm. It is observed that the saturation current decreases with increasing length of the gate. Indeed, the lateral extension of the space charge zone results in elongation of the conductor while thinning channel, limiting the passage of electrons.

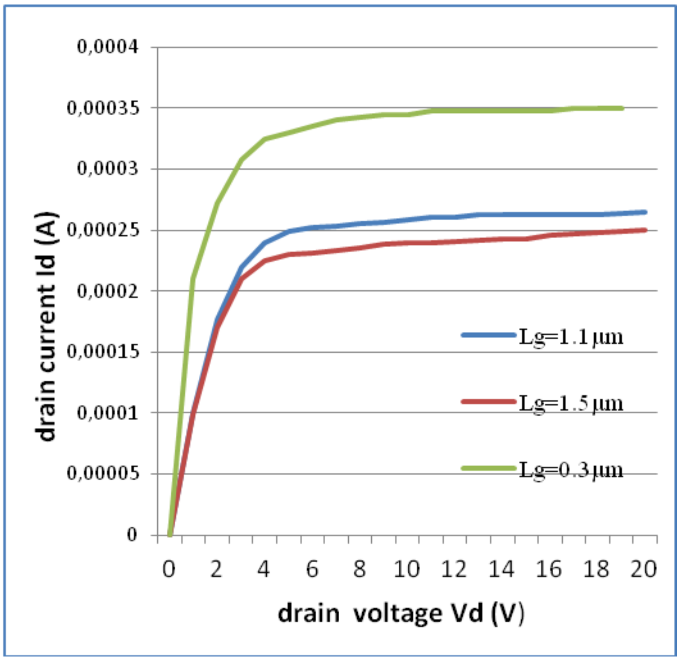

Fig14: Electrical Characteristic Id (Vd) of a MESFET (model 2) for different gate length Lg

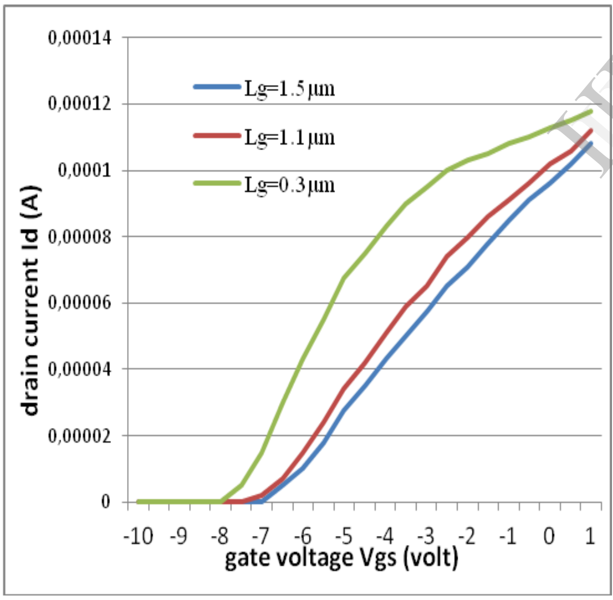

Fig15: Electrical Characteristic Id (Vg) of a MESFET (model 2) for different gate length Lg

COINCLUSION

Determining current in the channel of the MESFET is an important element in assessing the quality of transistor parameter because it directly affects the performance microwave

This study examines the effect of channel resistance on the electrical current. This resistance depends on the geometry of the MESFET; the gate length Lg, the thickness and doping of the active layer.

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ANNEX

$$C_{gs}=\frac{0.25C_{gs0}}{\sqrt{1-\frac{V_{new}}{V_b}}}.\left\{1+\frac{\left(V_{eff}-V_t\right)}{\sqrt{\left(V_{eff}-V_t\right)^2+d^2}}\right\}.\left\{1+\frac{\left(V_{gs}-V_{gd}\right)}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}+0.5\ .C_{gd0}\left\{1-\frac{\left(V_{gs}-V_{gd}\right)}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}$$

$$C_{gd}=\frac{0.25C_{gs0}}{\sqrt{1-\frac{V_{new}}{V_b}}}.\left\{1+\frac{\left(V_{eff}-V_t\right)}{\sqrt{\left(V_{eff}-V_t\right)^2+d^2}}\right\}.\left\{1-\frac{\left(V_{gs}-V_{gd}\right)}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}+0.5\ .C_{gd0}\left\{1+\frac{\left(V_{gs}-V_{gd}\right)}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}\right\}$$