# The Modeling and Simulation of Zero Voltage Switching, Power Factor Correction for Three Phase Three Level Boost Rectifier

Arpit Panchratan PG Student (Power Electronics) SATI VIDISHA(M.P.)

*Abstract* –The Three Phase Three Level ZVS PFC (power factor correction) Boost Rectifier for achieving low input current and low total harmonic distortion (THD) using four switches, zero voltage switching (ZVS). This SIMULINK model voltage stress across the four switches is one half of the output voltage. By using this also achieved low conduction losses. Line to line voltage use 340V which gave efficiency more then 96% and saw the less then 3% THD over the used input and above the 8-10% load range. Also achieved power factor correction.

Keywords: ZVS,ZCS, EMI, AC-DC convertor.

Abbreviations:  $C_c$ -Coupling capacitor,  $I_a$ , $I_b$  and  $I_c$  are inductor currents, $I_1$ , $I_2$  and  $I_3$  are input currents.

## [I]INTRODUCTION

Earlier the ZVS PFC THD DCM boost rectifier are introduced [4][5] that gives the idea to design the Simulink model. For achieving the high voltage performance by rectifier is not easily done, but analyzing the SIMULINK model, gave the performance the same by using soft switching.

This modal of the rectifier achieves less then 3% input current THD over the output voltage is above than 8-10% also. This model also performs automatically balance the output voltage because the series capacitor connected in load side. The advantage of the series connection of the output capacitors are performing either the single high voltage or two identical low voltages outputs given.

Capacitor connection of this way also shows "low cost high performance" components used in this model.

## [II] EMI FILTER

The Electromagnetic Induction (EMI) filter is the passive device which is used in this circuit for avoiding the noise at the time of fast high voltage transition performs.

The circuit of EMI filter given below

Mr. Sudhir P. Phulambrikar HOD (Electrical Dptt) SATI VIDISHA(M.P.)





EMI filter used hare for eliminating the unwanted noise signal which are super impose with the input current at the time of clamping in the circuit.

Hence transformer connects with the capacitor inductor topologies for handling the this type of input current

Transformer of the EMI is use to be same winding resistance and should be same voltage.

# [III] Three Phase three Level ZVS PFC THD boost rectifier by PWM (proposed system)



Fig-2 Proposed system for modal

The figure shows the three phase three level model of ZVS PFC BOOST rectifier proposed modal. In the circuit see the 3 phase input given to the EMI filter for avoiding the clamped noise. And then the input given to the Rectifier which is control by the four switches. Switches can be performed by the PWM method . Than the output of the rectifier is connected with the clamped capacitors' that connected in series. Connect the load across these capacitors and measure the output voltage.

#### [IV] The SIMULINK modal and Analysis

The three phase three level thd zvs pfc boost rectifier SIMULINK model shows in figure 3. In this model C1,C2 and C3 are the three capacitors connected in Y (star connection) and this connection create a neutral point. The virtual connection also connected with middle of pairs of switches and middle of output capacitors, which helps the balancing the output voltage.

By connecting the neutral point to the middle of the pair of switches, directly achieves the three input. Clamping capacitor  $C_c$  connected across the switch.  $C_{01}$  And  $C_{02}$  the out put capacitors. For clamped inductor take two winding linear transformer  $C_R$  capacitor use for reset the inductor current connected serially with pair of switches.

By figure 4(a) and (b) saw when the switch  $S_1$  and  $S_2$  on inductor current  $i_{L1}$  flows from inductor  $L_1$ ,  $S_1$  and  $S_2$  the  $i_{o1}$  flows through  $V_{o1}$  and switches capacitor  $V_{cc}$  will charged. After some time switch  $S_2$  will turned off then than the  $V_{cc}$  going to discharged and current flows from  $S_2$ ,  $S_3$ . the measured current peak of  $i_{L1}$  is equal to  $V_{AN}/L_1$ .

After some time the switch  $S_1$  also off. After some delay the switch  $S_3$  and  $S_4$  are on fig 4(c) and (d). This phenomenon actually for the negative half cycle for the rectifier. At this time current  $i_{L2}$  and  $i_{L3}$  flows through to the inductor  $L_2$  and  $L_3$  and also the current going to the  $V_{o2}$  side.

When the diode  $D_{C1}$  is forward biased than the current  $i_{L1}$  decreases linearly then the current calculated by equation,

$$i_{L1} = \frac{V_{AN} - (1 - 2D)V_{o1}}{2L_1}T_S$$

When the diodes  $D_{C2}$  and  $D_{C3}$  are forward biased than the current  $i_{L2}$  and  $i_{L3}$  are simultaneously increases linearly.

$$i_{L2} = \frac{-V_{AN} + (1 - 2D)V_{o2}}{2L_2}T_S$$

### [V] Switching for MOSFET

In the modal take the PWM method for switching performance. The figure-4 shows the switching phenomenon of the MOSFET When the S1 is ON then the S2 also ON for some instantaneous of time, then it will OFF.



Fig-5 Switching pulses for the MOSFET switches



Fig .3 The Three Phase Three Level Zvs Thd Pfc Rectifier Matlab Simulink Modal



Fig 4- analysis of the modal fig-4(a) and 4(b) for the switch operation of  $S_1$  and  $S_2$  and fig-4(c) and 4(d) for the switch operation of  $S_3$  and  $S_4$ 

After some delay the S4 switch will ON and at this time S3 will ON for some instantaneous of time and then it will be OFF.

# [VI] SIMULINK RESULTS

The results of the matlab simulink model was evaluated on  $340V_{L-L}$  voltage where the C1,C2 and C3 are  $2.2\mu$ F, L1, L2 and L3 are  $89\mu$ H.D1-D6 taking the simple ratings and the diodes D7 and D8 having high snubber value.



FIG.6 Input inductor current waveforms at full load  $340V_{L-L}$ 

Figure-6 show the input current  $I_{L1}$ ,  $I_{L2}$ , and  $I_{L3}$  waveforms of simulink result in scope at full power at  $340V_{L-L}$  voltage.



Fig.7 Measured DC out put at 340V<sub>L-L</sub> input voltage.

Figure-7 shows the output power at full load in voltage  $340V_{L\text{-}}$   $_{L}$  having 96% of efficiency .

Figure 8 shows the measured three level input voltage change by corresponding output voltage.

Figure 9 the three phase Input current  $(I_a, I_b, and I_c)$  THD of the input current achieved less then 3% total harmonics reduction level by the SIMULINK modal shows by figure-12.



Fig.8 Change in input voltage at full load



Fig.9 measured input current at full load

Figure- 10 and figure -11 shows Measured DC out put voltage at different switching operations like figure- 10 shows the  $S_1$  and  $S_2$  'ON' given the output DC voltage and Figure- 11 shows the  $S_3$  and  $S_4$  'ON' given the output DC voltage



Fig.10 Measured DC out put at S1 and S2 'ON'.



Fig.11 Measured DC out put at S3 and S4 'ON'.



Fig 12- THD of the Input current

## [VII] CONCLUSION

In this paper three phase three level ZVS THD PFC boost rectifier using four switch (PWM) simulink modal introduced . voltage across the each switch was clamped with output voltage (measured one half of its value). By SIMULINK results achieved less then 3% input current total harmonic distortion over the given input and achieved above 8-10% load.

The total performance done by MATLAB simulink at 340 line to line voltage .Achieved 96% efficiency with full load.

#### REFERENCES

- [1] M.H. RASHID POWER ELECTRONICS "ZERO VOLTAGE SWITCHING"
- [2] P Barbosa ,F.canales and F.C.Lee "Analysis an evaluation of the Two Switch Three Level Boost Rectifier ,"IEEE Power Electronics specialists' conf.(PESE) record ,2001,pp.1159-1164.
- [3] J.R. Pinheiro and I.Barbi,"The Three Level ZVS-PWM dc-dc converters ,"IEEE Transaction on Power Electronics .Vol8.No.4.pp.486-492,Oct. 1993
- [4] Y.Jang and M.M. Jovanovic, "The Taipei Rectifier a new three phase two switch zvs pfc dcm boost rectifier," IEEE Transaction on Power Electronics, Vol.28, No.2.pp.686-694, feb 2013
- [5] Y.Jang , M.M. Jovanovic and Juan M. Ruiz,"Three Level TAIPEI Rectifier ,"IEEE Transaction on Power Electronics,pp.943-950 April 2014.