Three Phase Bridgeless Interleaved Active Power Factor Correction Converter

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Abstract- In this paper, a new three-phase ac–dc bridgeless interleaved power factor correction topology is proposed for battery charging applications. The topology provides improved power factor and efficiency in comparison to conventional bridge rectifier topology, and leads to a decrease in charger size, charging time and hence, is cost effective. A detailed circuit operation for this topology is presented. Simulation results are included for a boost converter converting AC input voltage 230 V to 750 V DC output. Simulation results show an improved power factor and reduced THD, when compared to conventional topology. Power factor in proposed BLIL PFC is improved by 2.19% and THD is reduced by 26.25%.

Keywords: Bridgeless Interleaved, THD, Power Factor, Displacment factor, Distortion factor, MatLab.

1. INTRODUCTION

A Universal battery charger is supplied using an external power supply. The battery charger module as shown in fig.1 consists of AC and DC filters in line and load side respectively, an AC-DC Power Factor Correction (PFC) Boost converter is used for power factor correction which is followed by a DC-DC converter. A controller is used to control the charger set up. The AC-DC PFC boost converter is an important part in charger module. This AC-DC has to be selected carefully. For this a three-phase Bridgeless Interleaved (BLIL) PFC boost converter is proposed which will reduce the THD and increases the power factor.

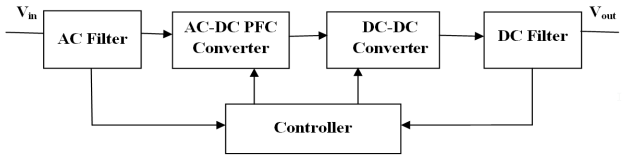

Fig.1. Block diagram of a universal battery charger

2. PROPOSED THREE-PHASE BLIL BOOST TOPOLOGY

The Three-phase BLIL PFC converter shown in Fig. 2 is proposed to overcome the problems in conventional converters. The proposed three-phase BLIL PFC Converter,consists of six MOSFETs, six diodes,six inductors and a capacitor parallel to load. A detailed converter operation a steady- state analysis is given in the following section

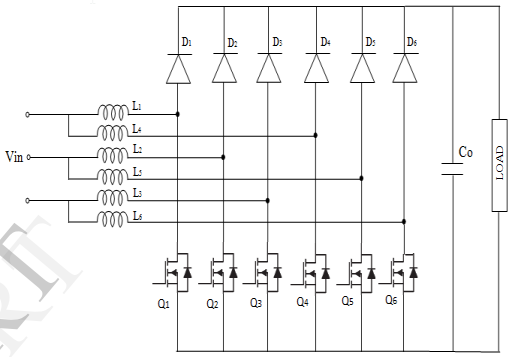

Fig.2. Proposed Three-Phase BLIL PFC Converter

3. CIRCUIT OPERATION AND STEADY STATE RIPPLE ANALYSIS

To analyze the circuit operation, the input line cycle has been separated into the positive and negative half cycles. Operation for each of the half-line cycles are explained in Sections 3.1 and 3.2 that follow.

3.1POSITIVE HALF CYCLE OPERATION

Referring to Fig. 2, during the positive half cycle, when Phase A and Phase B are conducting, Q_1/Q_2 turn on and current flows through L_1 and Q_1 and continues through Q_2 (and partially its body diode) and then L_2, returning to the line while storing energy in L_1 and L_2. When Q_1/Q_2 turn off, energy stored in L_1 and L_2 is released as current flows through D_1, through the load and returns through the body diode of Q_2 back to the input mains. With interleaving, the same mode happens for Q_4/Q_5, but with a 180◦ phase delay. The operation for this mode is Q_4/Q_5 on, storing energy in L_4/L_5 through the path L_4-Q_4-Q_5-L_5 back to the input. When Q_4/Q_5 turn off, en ergy is released through D_4 to the load and returning through the body diode of Q_5 back to the input mains.

During the positive half cycle, when Phase B and Phase C are conducting, Q_2/Q_3 turn on and current flows through L_2 and Q_2 and continues through Q_3 (and partially its body diode) and then L_3, returning to the line while storing energy in L_2 and L_3. When Q_2/Q_3 turn off, energy stored in L_2 and L_3 is released as current flows through D_2, through the load and returns through the body diode of Q_3 back to the input mains. With interleaving, the same mode happens for Q_5/Q_6, but with a 180° phase delay. The operation for this mode is Q_5/Q_6 on, storing energy in L_5/L_6 through the path L_5-Q_5-Q_6-L_6 back to the input. When Q_5/Q_6 turn off, energy is released through D_5 to the load and returning through the body diode of Q_6 back to the input mains. During the positive half cycle, when Phase C and Phase A are conducting, Q_3/Q_1 turn on and current flows through L_3 and Q_3 and continues through Q_1 (and partially its body diode) and then L_1, returning to the line while storing energy in L_3 and L_1. When Q_3/Q_1 turn off, energy stored in L_3 and L_1 is released as current flows through D_3, through the load and returns through the body diode of Q_1 back to the input mains. With interleaving, the same mode happens for Q_6/Q_4, but with a 180° phase delay. The operation for this mode is Q_6/Q_4 on, storing energy in L_6/L_4 through the path L_6-Q_6-Q_4-L_4 back to the input. When Q_6/Q_4 turn off, energy is released through D_6 to the load and returning through the body diode of Q_4 back to the input mains.

3.2NEGATIVE HALF CYCLE OPERATION

Negative half cycle operation is similar to that of the positive half cycle operation but the current flow direction will be in the opposite direction to that of the positive half cycle.

4. FINDING VALUES OF L AND C

Designing the values of L and C is very important. In the proposed BLIL PFC Converter the values of L and C are designed as follows.

Let us consider the instant when Phase A and Phase B are conducting. During this interval the voltage equation is given as

$$Vin=(L1+L2)\frac{\Delta iL1}{(1-D)Ts} \quad (1)$$

$$Vo-Vin=(L4+L5)\frac{\Delta iL4}{(1-D)Ts} \quad (2)$$

Assuming matched inductors, L_1, L_2, L_4 and L_5, the input ripple current is the sum of currents in L_1/L_2 and L_4/L_5

$$\Delta Iin=\frac{1}{L1+L2}Vo(1-D)Ts \quad (3)$$

From Equation 3

$$L1+L2=\frac{Vo(1-D)Ts}{\Delta Iin} \quad (4)$$

$$L=\frac{Vo(1-D)Ts}{2\Delta Iin} \quad (5)$$

At this interval the change in capacitor voltage ΔVc is given by

$$\Delta Vc=\frac{1}{C}\int_{t0}^{t1} Ic\,dt=\frac{1}{C}\int_{t0}^{t1} iL3\,dt \quad (6)$$

$$\Delta Vc=\frac{iL3}{C}(t1-t0) \quad (7)$$

$$\Delta Vc=\frac{iL3}{C}(1-D)Ts \quad (8)$$

From Equation 8

$$C=\frac{iL3}{\Delta Vc}(1-D)Ts \quad (9)$$

$$C=\frac{Vo*(1-D)}{\Delta Vc*f*R} \quad (10)$$

Where

$$Ts=\frac{1}{f}$$

$$iL3=\frac{Vo}{R}$$

R=output resistance

Equation 5 and 10 gives the value of L and C respectively.

5. SIMULATION RESULTS

5.1 CONVENTIONAL BOOST CONVERTER TOPOLOGY

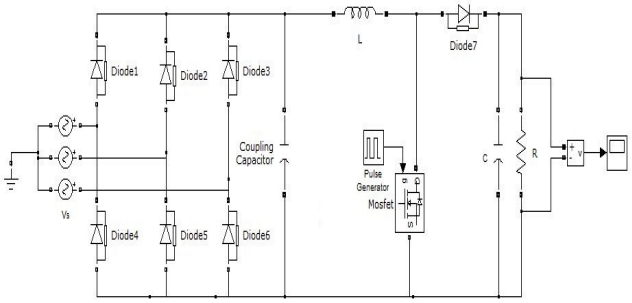

Fig.3. MATLAB Implementation of Conventional Boost Converter Topology

Design parameters:
Switching Frequency : 25 KHz
Input Voltage : 230 V

Output Voltage : 753 V
Duty Ratio : 0.67
Inductor : 131mH
Resistor : 200 Ω
Capacitor : 760µF

Fig.4 and Fig.5 shows supply voltage and supply current and THD plot waveform of a Three-phase Conventional PFC respectively for duty ratio 67%

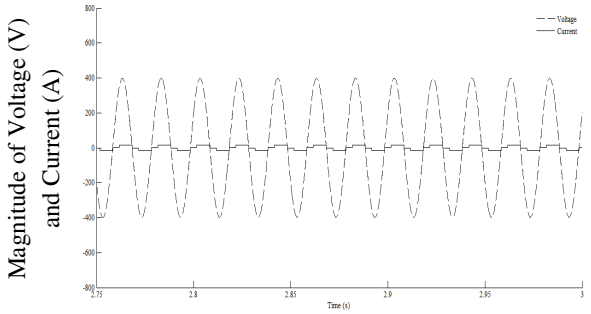

Fig.4 Supply Voltage and Supply Current waveforms

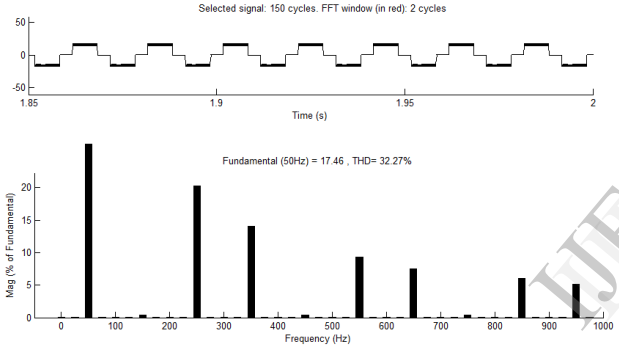

Fig.5 THD plot

Power Factor Calculation:
Formulas used:
Power Factor= $K_d * K_p$
$K_d = \cos\varphi$, $K_p = 1/\sqrt{THD^2}$
φ = Phase difference between input voltage and current
THD = Total Harmonic Distortion in input current
K_d= Displacement Factor
K_p= Distortion Factor

φ = 0.0017sec = 15.3°
Cos φ = Kd = 0.9645
THD = 32.27%
Kp = 0.9510
PowerFacto r = Kd * Kp = 0.9172

5.2 BRIDGELESS INTERLEAVED BOOST CONVERTER TOPOLOGY

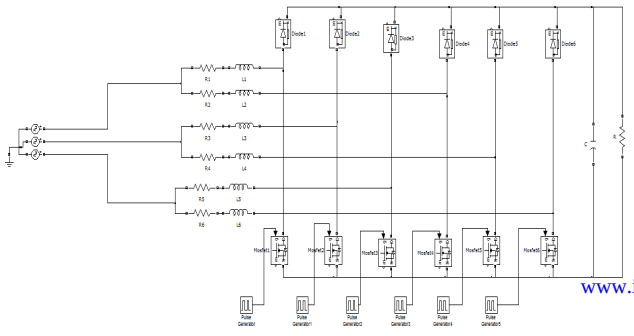

Fig.6. MATLAB Implementation of Bridgeless Interleaved Boost Converter Topology

Design parameters:

Switching Frequency : 25 KHz
Input Voltage : 230 V
Output Voltage : 757 V
Duty Ratio : 0.67/0.33
L1,L2,L3,L4,L5,L6 : 66.7 mH
Capacitor C : 975 µF
Resistor R : 200Ω
R1,R2,R3,R,R5,R6 : 25mΩ

DUTY RATIO: 67%

Fig.7 and Fig.8 shows supply voltage and supply current, THD plot and output voltage waveform of a Three-phase BLIL PFC respectively for duty ratio 67%

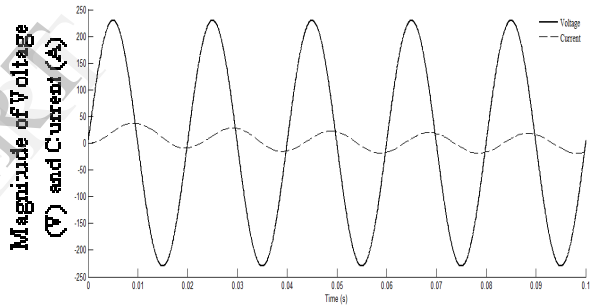

Fig.7 Supply Voltage and Supply Current waveforms

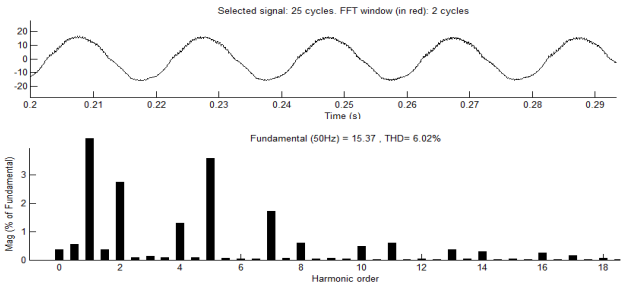

Fig.8 THD plot

Power Factor Calculation:

φ = 0.0022sec = 24.3^0
Cosφ = 0.9408
Kd = Cosφ = 0.9408
THD = 6.02%
Kp = 0.9982
PowerFactor = Kp * Kd = 0.9391

DUTY RATIO: 33%

Design parameters:

Switching Frequency	: 25 KHz
Input Voltage	: 230 V
Output Voltage	: 757 V
Duty Ratio	: 0.33
L1,L2,L3,L4,L5,L6	: 66.7mH
Capacitor C	: 975 µF
Resistor R	: 200Ω
R1,R2,R3,R,R5,R6	: 25mΩ

Fig.9 and Fig.10 shows supply voltage and supply current and THD plot waveform of a Three-phase BLIL PFC respectively for duty ratio 33%

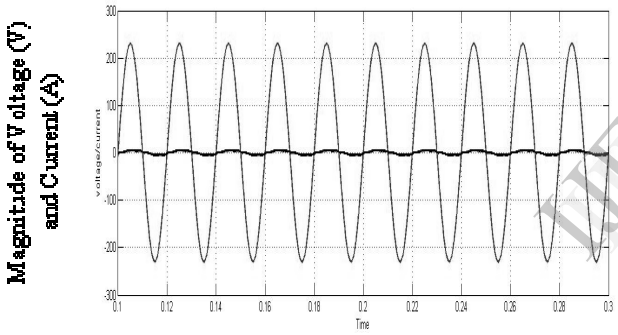

Fig.9 Supply Voltage and Supply Current waveforms

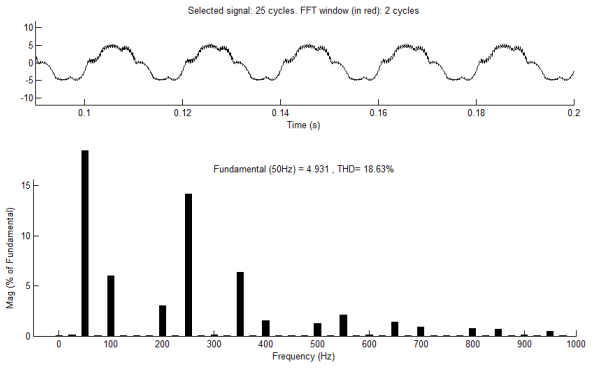

Fig.10 THD plot

Power Factor Calculation:

φ = 0.0025sec = 22.5^0
Cosφ = Kd = 0.9238
THD = 18.63%
Kp = 0.9830
PowerFactor = Kd * Kp = 0.9080

6. COMPARISON OF THD AND POWER FACTOR

Since, it is three-phase we have considered duty ratio as 67%. It is observed that the THD is reduced and the Power Factor is improved in proposed three-phase BLIL topology compared to three-phase conventional topology

TOPOLOGY	THD (%)	POWER FACTOR
Three-phase conventional (D=0.67)	32.27	0.9172
Three-phase BLIL (D=0.67)	6.02	0.9391
Three-phase BLIL (D=0.33)	18.36	0.9080

Table1. Comparison of THD and power factor

- Reduction in THD
  =32.27-6.02=26.25%
- Improvement in Power Factor
  =0.9391-0.9172=0.0219
  =2.19%

7. CONCLUSION

Thus from the above simulation results the following two were inferred. Duty ratio of 67% is best suited for three-phase converter topology. THD is reduced and Power Factor is improved in proposed three-phase BLIL PFC converter compared to Conventional topology.

8. REFERENCES

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