

Three Phase Parallel Multilevel Inverter Fed Induction Motor Using PD Modulation Scheme

N V Bharadwaj
Assoc. Professor
Member ISTE

B V Hemanth Kumar
Assoc. Professor

V Padmaja
Asst. Professor

Abstract

This Paper presents the Phase Disposition Scheme, which is topology independent. This scheme is used in Multilevel Inverters, interleaved parallel combination. Analysis on the other scheme which is Phase Opposition Disposition has also been performed. The best strategies related to the paralleling of inverters are evaluated, particularly those associated to current balancing between commutation cells of the same phase.

Pulse width modulation (PWM) strategies and methods for multilevel converters are usually developed for series converters. In this paper it is shown that they may be applied to parallel converters using interleaving techniques, given that these converters also have multilevel characteristics. PWM methods based on carriers' disposition and on zero sequence injection are studied for parallel multilevel inverters. Analysis shows that the best method in terms of load current ripple is the phase disposition method. The current balancing between commutation cells of the same phase is comparatively superior with this method. Another objective on which work was done was to analyze these problems and to propose a solution to cancel current imbalance when using PD strategy.

In addition to the above scheme POD (Phase Opposition Disposition) strategy has also been simulated which has shown comparatively same results as that of the PD strategy. The load was chosen to be a three phase induction motor drive and its parameters such as Stator Current, Speed and Electromagnetic Torque have been analysed as such.

I Introduction

Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly [1,2,3]. As a result, a multilevel power converter structure has been introduced as an alternative in high

power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters [4]. More recent applications have been for power system converters for VAR compensation and stability enhancement [5], active filtering [6], high-voltage motor drive [3], high-voltage dc transmission [7], and most recently for medium voltage induction motor variable speed drives [8]. Many multilevel converter applications focus on industrial medium-voltage motor drives [3, 9], utility interface for renewable energy systems [10], flexible AC transmission system (FACTS) [11], and traction drive systems [12]. The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages. However, the series connection of switching power devices has big problems [13], namely, non equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power

semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. Multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. Abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In this thesis sinusoidal pulse width modulation (SPWM) is used.

II Proposed Concept:

Multilevel conversion is not a priori limited to voltage source inverter (VSI), but three-phase drives are a huge market, and a lot of effort has been made to optimize the operation of multilevel three-phase VSI. In particular, modulation techniques have been thoroughly investigated, resulting to different options in using the zero sequence component of the reference as a degree of freedom. When it comes to comparing the performance of these different strategies, the approach presented is efficient.

As a first step, it is shown that different dispositions of the carriers are possible for multilevel converters. Then, it can be seen that, unlike other dispositions, phase disposition (PD) optimizes the line-to-line voltage because it makes carrier frequency harmonics as a common mode voltage that cancels out in the line-to-line voltage. For this reason, PD modulation is preferred to other dispositions.

The second benefit is that this carrier-based approach describes, within the same frame, conventional carrier-based strategies, space-vector modulation, and discontinuous modulations (only the variable frequency strategies, like hysteresis and sliding mode control, recalculated strategies, or direct torque control, are left aside). A point of interest is that the equation of the common mode component producing the same switching pattern as the multilevel centered space vector (CSV) strategy is given.

The third benefit is that this approach is topology independent, which was not always the case in previous literature. For example, it has been shown in how PD modulation can be applied to flying capacitor converters. Recently, the interest for parallel connection of commutation cell has grown. Depending on the application, increasing power, using standard modules, increasing the efficiency, or using smaller magnetic components can be the motivation, but due to the development of multilevel converters, interleaved switching is generally chosen or, at least, considered. Interleaving the switching signals of parallel cells reduces the output current ripple and increases the dynamic performance of the converter. However, the parallelization of a high number of commutation cells

using regular inductors to connect them is not recommended due to the increase of the current ripple in each cell. To solve this problem, coupled inductors may be used since currents in all cells are magnetically coupled, reducing their amplitude and increasing their frequency.

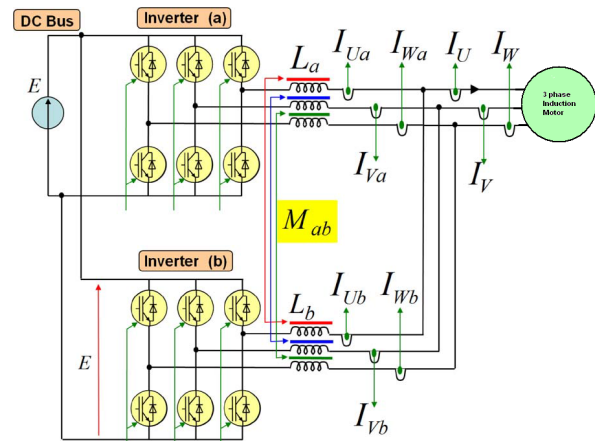


Figure 1. Three-phase parallel multilevel inverter

III Three-Phase Application Scheme:

The system to be analyzed is shown in Fig. 1. It is composed of two three-phase inverters connected in parallel. Each phase (U , V , W) is composed of two commutation cells (a and b) which are connected in parallel through coupled or uncoupled inductors. These inductors (L_a and L_b) have self-inductance L and mutual inductance M_{ab} . The load was chosen to be a three phase induction motor, which represent a machine. The aim of this paper is to present the way to adapt strategies developed for parallel multilevel converters.

IV Modulation Principle:

There are three reference signals shifted by 120° . They are imposed in an N -level system composed of $N - 1$ carriers. Each reference signal may have a sinusoidal waveform with or without a zero sequence signal. The modulation system generates three ideal waveforms obtained from comparisons for each of the three phases. Each output phase voltage has N levels. These ideal waveforms are sent to a second block which turns on and off the proper switches according to the required level.

The advantage of this type of approach is to comprise a first stage which is completely independent of the topology, and as a consequence, it can be studied and optimized separately. The second part allows us to adapt the generic modulator to the actual topology. For the first part of the modulator, various strategies are considered: phase opposite disposition (POD), or PD strategies. Consequently, a brief recall of the POD and the PD will be presented in order to emphasize the balancing behavior of two currents in parallel commutation cells. For this, we will focus on a significant variable related to the paralleling of

commutation cells: the current difference in each phase.

V Modulation System:

i. POD Modulation Scheme: For an N -level system, it comprises $N - 1$ vertically disposed carriers regularly shifted by 180° at N times the switching frequency (F_s) of the power switches. Thus, if the reference signal is at the top part (upper striped area), the output level is one. If it is inside the middle window (gray area), the output level is zero, while if it is at the bottom part (bottom striped area), the output level is -1 . The reference signal may be sampled at the carriers' frequency, i.e., at $2 * F_s$ for a three-level converter.

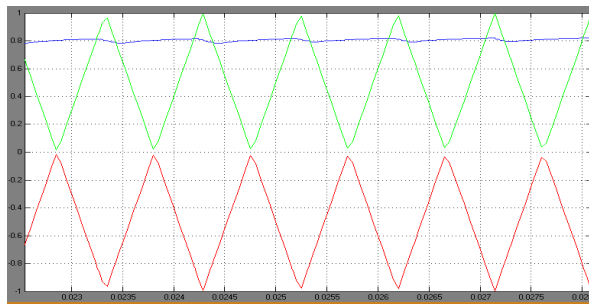


Figure 2. POD reference waveform

ii. PD Modulation Scheme: PD modulation in an N -level system consists of $N - 1$ vertically disposed carriers in phase. As in the *POD* modulation, if reference signal is at the top part (upper striped area), the output level is one, and if it is inside the middle window (gray area), the output level is zero. If it is at the bottom part (bottom striped area), the output level is -1 . The carrier frequency is also equal to $N - 1$ times the switching frequency, and in a three-level system, sampling occurs at $2 * F_s$.

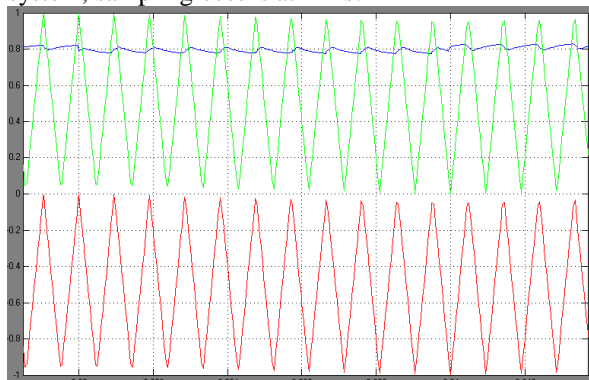


Figure 3. PD reference waveform

VI Current Difference Control:

With the intention to guarantee zero average current difference in each phase, it is essential to measure each of the two currents of each phase. In a classical multilevel modulation strategy, each cell is controlled by one modulator. The control is performed by adding a differential signal over both modulation signals. In our case, there is no separation of both modulation

signals since the commutation for each cell is assigned separately.

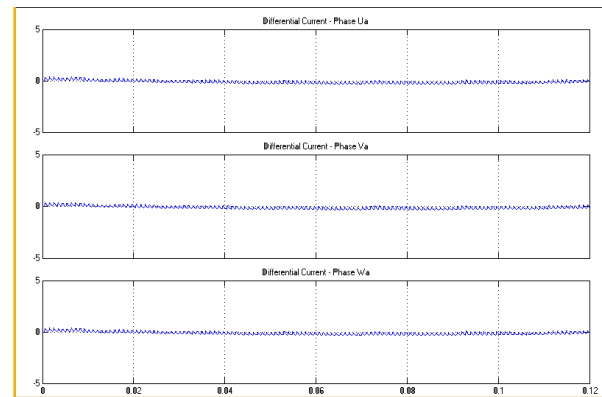


Figure 4. Three phase differential current

VII Simulation Results:

The simulation block in figure.1 shows the circuit with three phase induction motor load. The input voltage to the inverter cells is taken as 300V d.c. The mutual inductance values and the resistance values are taken accordingly. The corresponding output waveforms are as shown below.

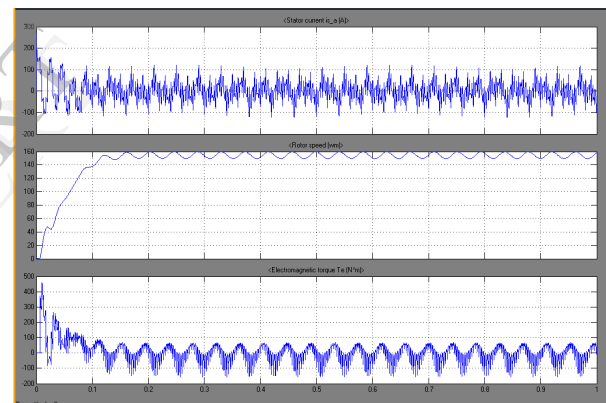


Figure 5. Stator current, rotor speed and E.M torque

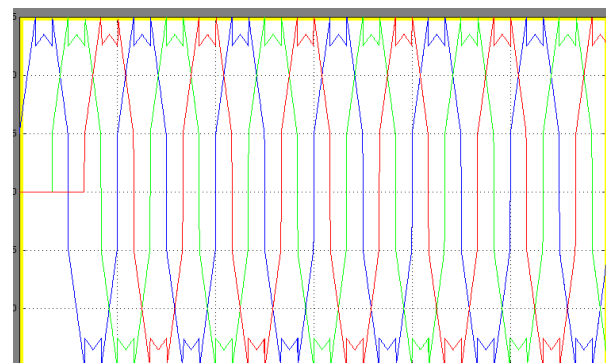


Figure 6. Three phase voltage waveforms of inverter

VIII Conclusion:

The work developed in this paper has shown that it is possible to obtain the best characteristics of both strategies by using the PD strategy coupled to a method which compensates the transitions of the

differential mode currents. It has been presented an active control of the differential mode current by adding a square waveform at the switching frequency, which removes the dc component of the differential mode current. This implies the need of measurement of the differential current and its comparison with a reference of zero current. PD modulation scheme has been successfully applied to an Induction Motor Drive.

References:

- [1] J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and application," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.
- [5] T. Meynard and H. Foch, "Multilevel choppers for high voltage applications," *Eur. Power Electron. J.*, vol. 2, no. 1, pp. 45–50, 1992.
- [6] G. Kalvenage and P. Aubin, "Sparc patent-power converter," *European Patent 02 290 258.9*, Feb. 4, 2002.
- [7] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna PowerTech Conf.*, 2003, pp. 1–6.
- [8] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [9] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [10] T. Meynard, "Overview of multilevel converters and applications," in *Proc. ECPE Workshop Adv. MultiLevel Converter Syst.*, Vasteras, Sweden, 2010, pp. 34–35.
- [11] J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 412–420, Feb. 2011.
- [12] B. Cougo, T. Meynard, F. Forest, and E. Labouré, "Optimal PWM method for flux reduction in intercell transformers coupling double three-phase systems," in *Proc. Conf. Electron. Puissance Futur*, 2010, pp. 1–6.
- [13] B. P. McGrath and D. G. Holmes, "An analytical technique for the determination

of spectral components of multilevel carrier based PWM methods," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 847–857, Aug. 2002.

[14] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, Sep./Oct. 1998.