Threshold Logic Computing: Memristive-FinFET Circuits for FFT & Vedic Multiplication

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***Abstract*—Threshold logic computing is the simplest kind of computing units used to build artificial neural networks. Brain mimic circuits can be developed electronically in different ways. But using Memristive Threshold Logic (MTL) cells have various advantages than Logic gates. MTL cell is used for designing FFT computing useful for signal processing applications and Vedic addition and multiplications for efficient Arithmetic Logic unit design. MTL cell is the basic cell which consist of two parts: Memristor based input voltage averaging circuits and an output threshold circuit. The threshold circuit is the combination of Op-amp and FinFET circuit. FinFET circuits indicate much lower power consumption, lower chip area and operates at lower voltages.**

Keywords—FinFET circuits; Memristor; Threshold logic; FFT ; Vedic multiplier.

I. INTRODUCTION

By Moore's Law, the computational power of computers is increased with reduction in their size and power consumption. Thus many new commercial products have been developed. So, Moore's law cannot be continued for longer periods, a different architecture might be needed to continue to make sizable jumps in computer development.

Memristor is used in our new technology. Recent progress in memristive devices has gained interest in neuromorphic computing architectures. The memristor- Fin-FET can realize low-power circuits with increased reconfigurability and smaller physical layout area. Hybrid memristive-FINFET circuits can be used for logic implementation of Threshold logic gates (TLG).

VLSI implementations of brain like logic gates can be used to mimic neuron activity of brain functionally and electrically [1]. But this implementations have certain limitations related to the scalability of networks and solving large variable Boolean logic problems. So many works are in progress related to the possibility to mimic the brain like circuits and logic gates. Mimicking brain like circuits can be done in two ways; (i) Designing conventional computational blocks by applying threshold logic gates. (ii) Developing a completely trainable architecture without strictly following computing topologies.

Threshold logic is the primary logic of human brain that inspires from the neuronal firing and training mechanisms. It also represents a general theory of switching functions [2].while threshold logic offers powerful computational properties beyond Boolean logic, threshold logic applications in CMOS and other bulk semiconductor technologies are expensive because of their area, power, and delay overhead. In the beginning stage, threshold gates have been implemented using CMOS devices, Single Electron Transistors and Monostable-Bistable Logic Elements and resonant tunnelling diodes. Capacitor-based Threshold Logic gates (CTL) are implemented using capacitors as weights along with CMOS-based comparator circuits. In CMOS CTL gates, sum of weighted input voltage is compared with a fixed reference voltage, and based on this comparison, a logical output is produced. CTL gates are used for 2D image filtering in. These CTL gates have many advantages such as low power, high resilience to process variations and feasibility for large circuit implementations.

The CMOS based circuits have limited scaling ability. Due to the scaling limitation short channel effect will arises. The short channel effect leads to the more power consumption and delay will also be increased. To overcome these drawbacks FinFET based circuits can be introduced. These circuits can operate at lower supply voltage.

This paper proposes a memristive threshold logic cell for brain mimicking to design conventional computing blocks. The MTL cell shown in Fig.1 is the basic cell, which consists of two parts: 1) a memristor based input voltage averaging circuit and 2) an output threshold circuit. The threshold circuit is the combination of operational amplifier and FinFET circuits.

FinFET technology has recently seen a major increase in adoption for use within integrated circuits [3]. The FinFET technology promises to provide the superior levels of scalability needed to ensure that the current progress with increased levels of integration within integrated circuits can be maintained. The FinFET offers many advantages in terms of IC processing that mean that it has been adopted as a major way forwards for incorporation within IC technology.

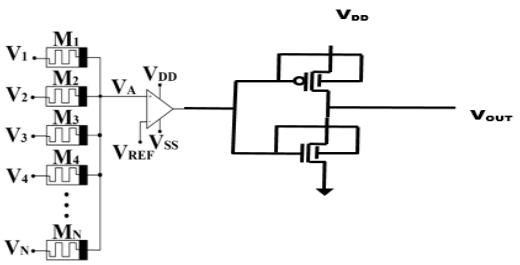

Fig. 1. MTL Cell.

II CIRCUIT DESCRIPTION

A.MEMRISTOR

A memristor is a two-terminal electronic device whose conductance can be precisely modulated by charge or flux through it [4]. A nanoscale silicon-based memristor device is a hybrid system composed of complementary metal-oxide semiconductor neurons and memristor synapses, which can support important synaptic functions such as spike timing dependent plasticity. A memristance naturally arises in thin-film semiconductors for which electronic and dopant equations of motion are coupled in the presence of an applied electric field Using memristors as synapses in neuromorphic circuits can potentially offer both high connectivity and high density required for efficient computing.

The structure of Memristor includes thin film of titanium dioxide (TiO_2) sandwiched between two platinum terminals. The titanium dioxide layer is doped on one side with oxygen vacancies, TiO_{2-x}. The doped region has lower resistance than that of the insulated undoped region. The boundary between doped and undoped region determines the effective resistance of the device. Let D be the total width of the TiO_2 layer and W be the width of the doped TiO_2 layer.

When a positive voltage is applied at the doped side, the oxygen vacancies move toward the undoped region, increasing the width of the doped region, W and hence the effective resistance of the memristor decreases. The effective resistance M_{eff} of the memristor is ,

$$M_{eff} = (W/D)R_{ON} + (1 - (W/D))R_{OFF} \quad (1)$$

where R_{ON} (=1 k) is the resistance of the memristor if it is completely doped, and R_{OFF} (=100 k) is the resistance of the memristor if it is undoped. When input voltage is withdrawn or when there is no potential difference between the terminals, the memristor maintains the boundary between the doped and undoped region, since the oxygen ions remain immobile after removal of the input voltage. Thus, the resistance will be maintained at the same value before withdrawing the input voltage. From the equation,

$$i = v/M(q) \quad (2)$$

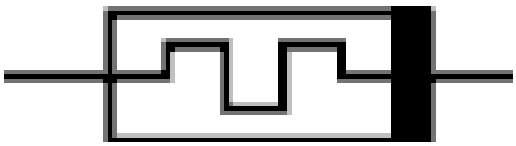

Fig. 2. Symbol of Memristor

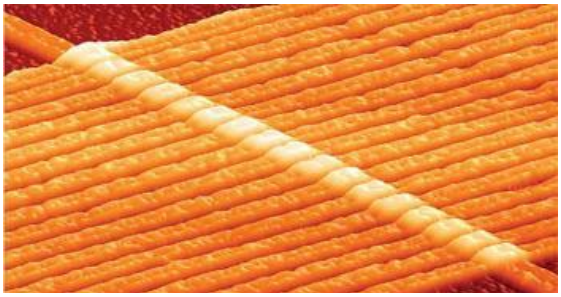

Fig. 3. Nano-sized Memristor

where v and i are the voltage and current across the memristor, and $M(q)$ is charge dependent resistance of the memristor, we can see that when the voltage difference across the memristor is 0, the current through the memristor is 0. If there is reverse potential across the memristor, the width of the undoped region increases, resulting in an increase in the effective resistance of the memristor. This high resistance will block the reverse leakage current through the memristor, when the number of inputs increases, the collective forward current through the circuit does not increase significantly, since the effective resistance in the memristor is constant.

B. Fin-FET

FinFET devices are a kind of special quasi-planar double gate (DG) devices and can be used as promising substitutes for the bulk CMOS devices at and beyond the 32nm technology node. FinFET devices have properties such as lower gate leakage, stronger gate control, reduced short-channel effects, and less performance variability compared to bulk CMOS counterparts [3], [5]. Because of these superior characteristics, FinFET devices show significant advantages in terms of performance and energy consumption for sub/near-threshold designs, and allow for higher voltage scalability. Due to the transistor-width quantization effect, i.e., wider FinFET transistors are formed by utilizing multiple parallel connected fins with the same height, sizing of FinFET devices is quite different from that of bulk CMOS devices. However, the characteristics of FinFET devices in the sub/near-threshold region are significantly different from those in the conventional strong-inversion region.

A FinFET device has a double-gate structure, in which each fin contains two equivalent gates: a *front gate* and a *back gate*, as shown in Fig. 5. Each fin is essentially the

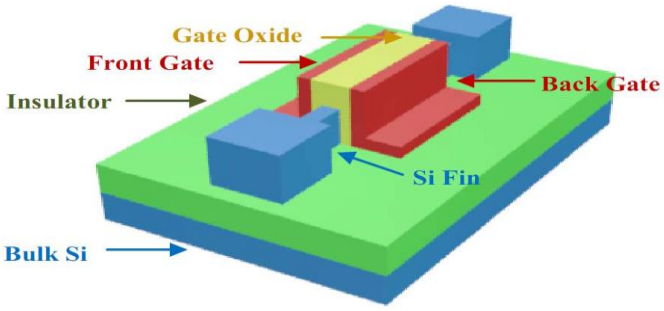

Fig. 5. Double-gate FinFET device structure.

parallel connection of the *front-gate-controlled* FET and the *back gate-controlled* FET, both with width W equal to the height of the fin. A Fin-FET device can be worked in two

possible modes: the *double-gate mode*, where both the front and the back gates of the fin are tied to the same control signal, and the *independent-gate mode*, where the front and the back gates are tied to different control signals. Due to the capacitor coupling of the front gate and back gate, the threshold voltage of the front-gate-controlled FET varies in response to the back-gate biasing voltage, and vice versa. Within a relatively small range of the back-gate biasing voltage, a linear relationship is observed between the change of the threshold voltage and the back-gate biasing voltage.

III COMPUTING CIRCUITS WITH THRESHOLD LOGIC

A. Memristive Threshold FFT Circuit

Fast Fourier Transform (FFT) is one of the most efficient algorithm widely used in the field of modern digital signal processing to compute the Discrete Fourier Transform (DFT). FFT is used in everything from broadband to 3G and Digital TV to radio LAN's [6]. Due to its intensive computational requirements, it occupies large area and consumes high power.

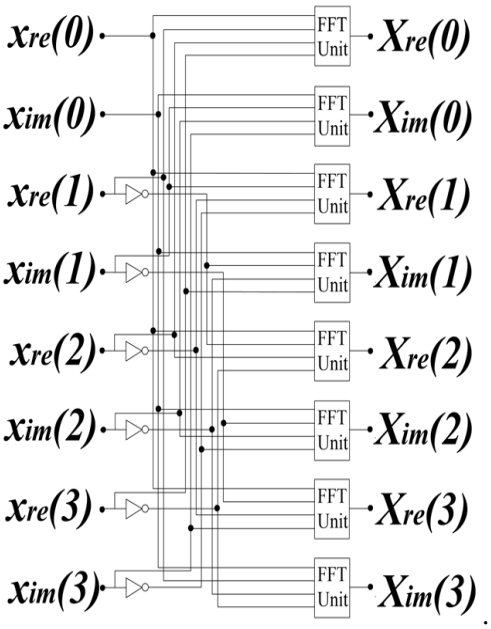

Fig .6. Block diagram of a four-point DFT processor.

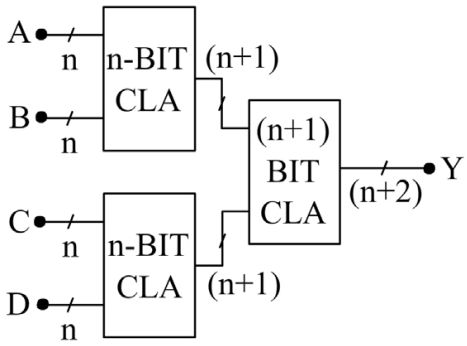

Fig. 7. Block diagram of FFT units used in the DFT processor.

FFT unit consists of four inputs and one corresponding FFT output. Inputs are given to the FFT units. The inputs, which are to be subtracted, are applied in such a way that which are complemented and added [7]. The real part and the imaginary part of the first output in four-point FFT requires only addition operation. Hence, the inputs to the first two FFT units in Fig. 6 are not complimented. These FFT units are implemented using 3 carry-look ahead adders (CLAs) as shown in Fig. 7. Other than the first two FFT units, rest of the six FFT units have two additions and two subtractions. Inputs to be added are given to the first CLA, whereas the inputs that are to be subtracted are complimented and then added using the second CLA. To obtain the twos compliment, 1 is to be added to the least significant bits (LSBs) of inverted inputs. For this, we utilize the *C*0 pin of the CLAs and a logic high is applied to the *C*0 pin of both the 8-bit CLA. This operation equates to adding one twice. Now, the outputs of these CLAs are added using the third CLA whose output result in the required transform. The CLAs are implemented using the proposed MTL circuits.

B. Memristive Threshold Vedic multiplier

Multiplication is a critical operation of Digital Signal processing (DSP) applications (like DFT, FFT, convolution etc), Arithmetic and logic unit (ALU), and multiply and Accumulate (MAC) unit (which is basically a multiplier itself). High Speed Multiplication is thus an essential requirement to increase the performance of processor [8]. The basic multiplication is performed using one of the techniques of Vedic Mathematics, and the accumulation of partial products is done using a specific design. Both the design and the vedic technique, results in a high speed multiplier. Vedic Mathematics is based on 16 sutras, out of which, "Urdhva triyagbhyam" sutra is used. In this technique intermediate products are generated in parallel,that makes multiplication faster.

Urdhava Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Tiryakbhyam. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the

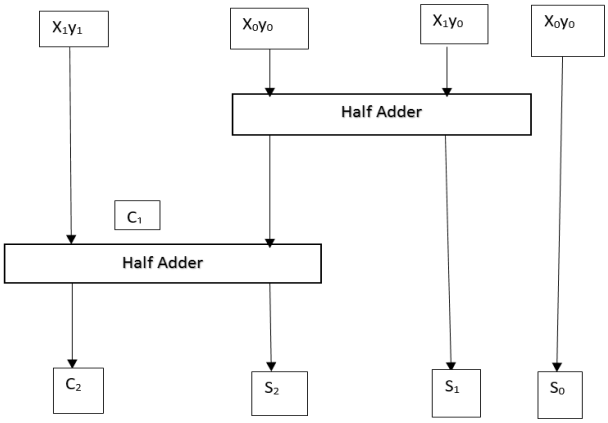

Fig.8. Architecture of 2*2 multiplier

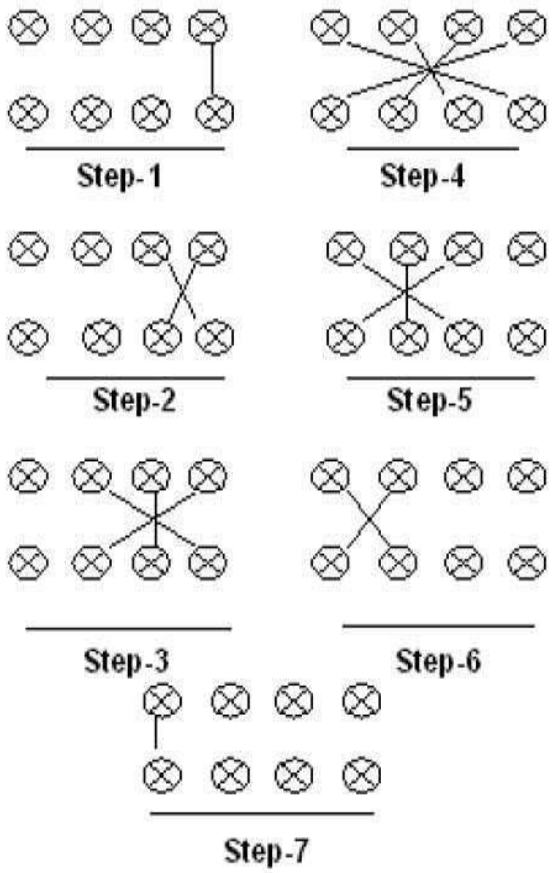

Fig. 9. Line Diagram for multiplication of binary numbers

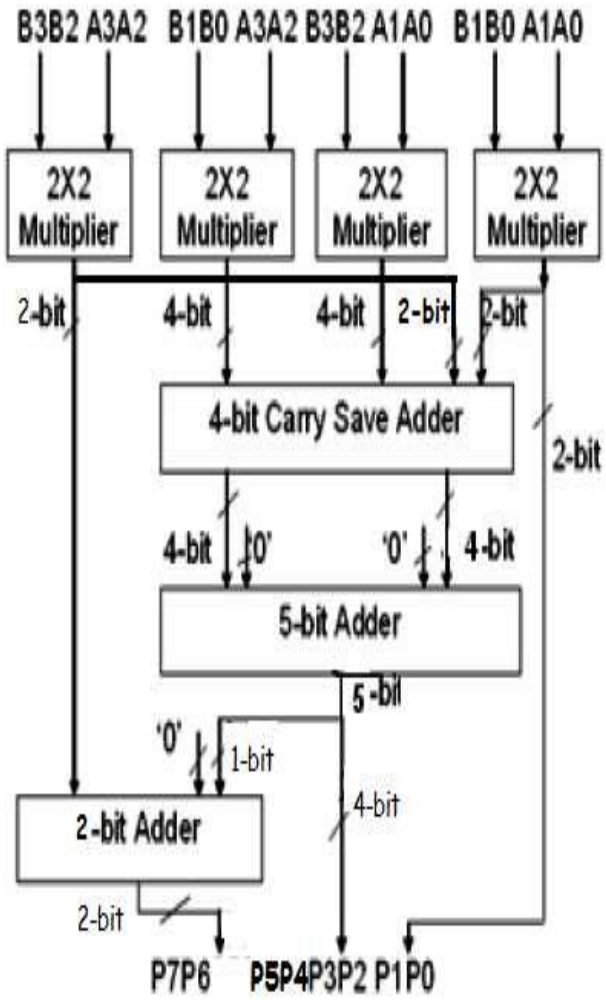

Fig.10. Architecture of 4*4 multiplier

number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient.

The 2*2 Multiplier Architecture is obtained by using 2 half adders and four and gates, as shown in Fig.8 [9] .The product X0Y0 is directly given to the output. X1Y0 and X0Y1 are added using first half adder, sum is given directly to the output and carry is added with product X1Y1 using second half adder.

The architecture of 4*4 Multiplier consists of four 2*2 Multipliers, a 4-bit carry save adder, a 5-bit adder, and a 2-bit adder as shown in Fig. 10. This design performs the accumulation of partial products in such a way, that it reduces the delay, compared to other multipliers, and along with those partial products is generated in parallel, so delay is further reduced. The least significant two bits of the first 2*2 multiplier are directly given to the output as output bits P1P0. The most significant bits of the output of the same multiplier are concatenated with the least significant two bits of the fourth multiplier, and the resulting value is added with 4-bit outputs of the second and third multiplier using carry save adder. The sum and carry output of carry save adder are added using a 5-bit adder. The least significant four bits obtained as output of the 5-bit adder are given at the output as

P5P4P3P2. And the most significant 6th bit is appended with 0 and added with the most significant two bits of the fourth multiplier using 2-Bit adder, the result is given as P7P6 bit of the output.

The total critical path delay is equal to the delay of 3 Full adders and 6 half adders. In the similar manner, we can implement designs of 8*8 and 16*16 multipliers, using four 4*4 and four 8*8 multipliers respectively.

IV CONCLUSION

In this paper, an improved memristor-Fin-FET threshold logic cell having lower-power dissipation and smaller on-chip area and high operational speed is proposed. In comparison with Memristive CMOS Circuits, Memristive- FinFET Circuit has lower chip area, low power consumption, high operational speed and also operates at lower voltages. Here, the notion of the brain mimicking is restricted to develop a generalized memristive threshold logic (MTL) cell in application to designing conventional computing blocks. Furthermore, this brief reports the successful application of the MTL cells in the examples of FFT and Vedic multiplication computing circuits.

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REFERENCES

[1] Alex Pappachen James, Dinesh s. kumar and Arun vijayan, "Threshold Logic computing: Memristive- cmos circuits for FFT and Vedic multiplication'', Nov.2013.
[2] Ramesh Karri, Jeya Vijayan Rajendran, and Harika Manam, "An energy efficient Memristive Threshold Logic circuit'',IEEE Trans. Computers vol-61 no.4 April. 2012.
[3] S.Priyanka, P.Deepa and V. M. Senthil Kumar, "Design of an adiabatic Fin-FET Circuit Operating in medium strong inversion region'', vol.4 Issue 11 Nov.2015.
[4] L.O.Chua," Memristor-The Missing Element'', IEEE Trans. Circuit Theory,vol CT -18, no.5 pp 507-519 sep.1971.
[5] XueLin, Yanhi Wang and Massud Pedaram ,"Stack Sizing Analysis and optimization for Fin-FET logic cells and and circuits operating in the sub/ near Threshold region''.
[6] Dr.S. Jayanthy and Belma Josephy ," Design of High speed FFT Processor'',vol.4 ,Issue 4 April 2014.
[7] K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation. New York, NY, USA: Wiley, 2007.
[8] B. K. Tirthaji, Vedic Mathematics. Jawahar Nagar, India: Motilal Banarsidass, 1965.
[9] R. Pushpangadan, V. Sukumaran, R. Innocent, D. Sasikumar, and V. Sundar, "High speed vedic multiplier for digital signal processors," IETE J . Res.,Vol .55