Thyristorised Real Time Power Factor Correction (TRTPFC)

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Abstract

One of the concerns to put on the energy efficiency is in relation to the system power factor. From the view of industrial practices, low power factor might cause equipment failure and higher operation costs. This paper proposes a conceptual design of microcontroller based automatic power correction (APFC Relay) for $1 - \phi$ and $3 - \phi$ circuit with intension to be used in power factor (either linear or non-linear) loads applications. The design of this auto adjustable power factor correction is to ensure the entire power system always preserving almost unity power factor and thus optimizing the current consumption and compared with predetermines reference value. The conceptual design of power factor correction techniques has gone through a set of simulation tests using Power System Computer Aided Design (PSCAD). The results are obtained and verified that the proposed PSCAD circuit is capable to produce a reliable output and can be further be implemented in practical application.

Keywords: Energy Saving, Reduction of Harmonics, Power Factor Correction

1. Introduction

All Power factor is the relationship between working (active) power and total power consumed (apparent power). Essentially, power factor is a measurement of how effectively electrical power is being used. The higher the power factor, the more effectively electrical power is being used. Low power factor means poor electrical efficiency. The lower the power factor, the higher the apparent power drawn from the distribution Network.

When low power factor is not corrected, the utility must provide the nonworking reactive power IN ADDITION to the working active power. This results in the use of larger generators, transformers, bus bars, wires, and other distribution system devices that otherwise would not be necessary. As the utility's capital expenditures and operating costs are going to be higher, they are going to pass these higher expenses to Industrial users in the form of power factor penalties [1-4]. One of the new approaches is to use a variable inductor in parallel with a fixed capacitor as a reactive power compensating circuit [5]. The inductor current is controlled by adjusting the firing angle of two antiparallel connected thyristors or using TRIAC. The adjustment of the thyristors' firing angle is made in Accordance to the result of a comparison between the measured values of a certain system parameter with its reference value [6].

This paper proposes a real time power factor correction scheme for $1-\emptyset$ and $3-\emptyset$ system. The selection of the capacitor according to load value and simulation for both systems with harmonics are including in this paper.

2. Block diagram of $1 - \emptyset$ system:

The figure shows the block diagram of the $1 - \emptyset$ power factor correction system. There are two references namely Voltage and Current measured from the PT and CT. These two references are compared and their resultant angle is given as firing angle of Thyristor. Before them these references are gone through the band pass filter and zero crossing detector. ZCD converts the sinusoidal waveform into square waveforms for triggering thyristor at every zero crossing.



Figure 1. Block Diagram of 1 - Ø System



In figure 1, i_s is the Source current; Vs is the Source voltage; i_1 , i_2 , i_3 are the load current, Capacitive branch current, Inductive branch current respectively. Figure 2 and 3 are theoretical waveforms of the $1 - \emptyset$ system. I_s and V_s are the output current and voltage of the ZCD respectively.



Figure 3. Waveform of legging pf

2.1 Circuit Diagram of 3-ø System



Figure 4. Block Diagram of 3 - Ø System

This figure 4 seems that power circuit diagram of RTPFC panel. This control circuit will control the load power factor by sensing various parameters like switching devise thyristor, inductors, capacitor banks etc. And generally this will have one incoming switch like MCB. In this figure 4 3- Ø supply is given through MCB and C.T is connected to the line which is measured the current, And secondary terminal of C.T is connected in terminal (s1 and s2) of APFC relay's terminal (YL and YM).Phase angle will be measured by pick controller in APFC relay which is given to the zero crossing device. And this thyristor switched devise TRTPFC is switch at zero crossing device. Power factor correction is the process of compensating for the lagging current by creating a leading current by connecting capacitor in parallel to the supply.

3. Simulations and Results:

The following figure shows the power circuit diagram of the $1-\emptyset$ system. The anti parallel connected thyristors are used as the control element for the p.f. correction.



Figure 5. Power Circuit of 1 - Ø System

The following figure shows the control circuit for the $1-\emptyset$ system. There are two references which are compared and the angle difference is given as the firing angle for one thyristor and 180° phase shift phase angle for the other thyristor.



Figure 6. Control circuit of 1 - Ø System

The following figure shows the simulated waveforms for 1– \emptyset system. In figure 7, V_{rms} and I_{rms} are the voltage and current of system respectively which are equivalent to theoretical waveforms (Figure 2). G1 and G2 are the gate signals for anti parallel connected thyristors or TRIAC. E₀ and I₀ are the simulated output waveforms of the 1 - \emptyset system.



Figure 7.Waveforms of 1 - Ø System

The following figure shows the control circuit diagram for Harmonics analysis of $1 - \emptyset$ system.



Figure 8. Control circuit of 1 - Ø System with Harmonics





Figure 9 shows the harmonics are present at source side and after applying the TRTPFC control technique for nonlinear load, all higher order load harmonics are eliminate effectively.



Figure 10. Power Circuit of 3 - Ø System



Figure 11. Control circuit of 3 - Ø System

The following figure shows the control circuit diagram for $3-\emptyset$ system. In $3-\emptyset$ system, phase angle for each phase is given at 0° , 120° and 240° . The value of capacitor is depending on the value of load. So, selection of the capacitor value is based upon following relation.

KVAR of Capacitor = $P \times (Tan \Phi 1 - Tan \Phi 2)$

Where P is value of load in kW Φ1 is actual angle between Voltage and current Φ2 is required angle between voltage and current

Per phase capacitance
$$KVAR = \frac{KVAR}{3}$$

$$\operatorname{Icph} = \frac{Vph}{Xc} = \frac{Vph}{\frac{1}{2\pi fC}} = \operatorname{Vph} x \ 2\pi fC$$

KVAR/ Ph =
$$\frac{Vph Iph}{1000}$$

After simulating $3 - \emptyset$ circuit as shown in figure-10. Following results are obtained. As in figure-12 .3- \emptyset input voltage, input current, output voltage, output current and voltage is nearly same as input voltage and current.



Figure 12. Control circuit of 3 - Ø System

The following figure shows the gating signals for $3 - \emptyset$ system.



Figure 13. Waveforms of Gate signals of 3 -Ø

The figure -14 shows the control circuit for $3 - \emptyset$ system for Harmonics Analysis.



Figure 14. Control circuit of 3 - Ø System with Harmonics

The following figure shows the harmonics waveforms for $3-\emptyset$ system.



Figure 15. Waveforms of 3 - Ø System with Harmonics

Figure-15 shows the harmonics are present and load harmonics are effectively eliminated by applying TRTPFC control technique.

4. Conclusion

PFC preregulators are needed to improve output voltage dynamics. In under load condition, voltage leads the current due to capacitive effect and in overload condition; system draws more current due to inductive effect that produces the harmonics. By using TRTPFC technique, that improve output voltage and eliminates the harmonics which shown in simulation results. TRTPFC also improves the power factor almost to unity which saves the energy. TRTPFC technique is easily implemented in practical system.

5. References

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