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Transformerless High Gain Boost Converter for Low Power Applications with Feedback Control

Mr. Md Yaseen
PG Scholar, M.tech (Power electronics)
EEE Department,
Dayananda Sagar College of Engg.
Bangalore, India

Dr. P. Usha
Professor, EEE Department,
Dayananda Sagar College of Engg.
Bangalore, India

***Abstract*—Atransformer-less boost converter which provides high voltage gain without utilizing transformer or coupled inductorsandextreme duty cycle is proposed in this paper. Also it is able to cancel the ripples in the input current at a preselected duty cycle, without increasing the number of components.The converter combines the features of boost converter and a three switch high voltage converter. At the input side, two inductors are interleaved for cancelling the input current ripple and at the output side switched capacitor voltage multiplier is used to increase the voltage gain. Feedback control is used to make the output voltage constant in spite of variation in the input or load or both i.e. both line and load regulation is accompanied. This proposed converter configuration helps eliminate the input current ripple and voltage deregulation for low power applications.**

Keywords—High gain boost converter, input current ripple cancellation, line and load regulation.

I. INTRODUCTION

Renewable energy sources are gaining momentum for the generation of electricity due to the rapid depletion of fossil fuel reserves. Also continuous consumption of traditional fossil energy sources leads to global warming.The voltage obtained from these renewable energy sources is usually low in amplitude; hence a boost converter is needed to step up the voltage to the required level and alsoto drain a continuous current with minimum ripple. Line and load regulation is also an important factor in the low power applications. Therefore this converter is more feasible for these applications.

Several other topologies have been proposed which includes the use of a coupled inductor and/or transformer, switched capacitor converter, zeta converter, bridge converter etc.

The use of couple inductors sometimes induces high voltage spikes across the switch, because of the resonance between leakage inductance and parasitic capacitance which is caused by the leakage inductance energy [1]. A clamp circuit is used to recycle the leakage inductance energy in the coupled-inductor boost converter reducing the voltage stress on the switch [2]. In the capacitor-diode clamped circuit, the leakage energy is recycled in the similar way without utilizing an additional switch [3]. The use of ZCS and/ ZVS technique with coupled-inductors and transformers is presented in [4]. In this switches turned on at zero voltage and turned off at zero current. The paper presented in [5], uses coupled-inductor and voltage lifting technique to achieve a high voltage gain. In [6], a switched coupled-inductor boost converter is presented where the leakage energy is recycled by a series diode in parallel with the basic boost converter diode. The converter presented in [7] uses coupled inductor and switched capacitor technique for a flyback converter. The coupled-inductor transfers the energy to load or capacitor and leakage energy is recycled. The switched-capacitor increases the voltage gain. Similar technique is used in [8].The converter in [9] is a non-isolated high gain boost converter based on half bridge converter; it combines features of boost converter and a half bridge converter with voltage doubler rectifier. In [10] and [11] integrated coupled-inductor and voltage doubler technique is used to achieve a high voltage gain. Converters with only switched-capacitors (without coupled-inductors) are suitable for low power applications mainly because of switching frequency limitation and current spikes in the capacitors. Converters presented in [12] and [13] which are based on Switched-capacitor achieve a high voltage gain. For high power applications, converters which do not use transformer or coupled-inductor are presented in[14], [15], and [16] which are based on switched-capacitor concept. Switched-capacitor with complete charge interchange presented in [17], is not used in voltage regulation since it compromises the converters efficiency. Switched-capacitor with complete charge interchange and Pulse width modulation presented in [18] provides voltage regulation. In renewable energy applications, converter must also drain continuous current with minimum ripple in the current.

The proposed converter combines complete charge interchange – switched capacitor with a boost converter into a single converter. Herein, the input current ripple is removed by interleaving two inductors at the input side and voltage gain is increased by using switched-capacitor multiplier at the output. A small inductor is used to limit the peak current due to switching process which minimizes the current spikes in the circuit. Feedback control is used to control the duty ratio of the switches make the output voltage constant in spite of variation in the input or load or both i.e. to provide both line and load regulation.

II. DESCRIPTION OF THE PROPOSED CIRCUIT

The circuit diagram of the proposed converter is shown in Fig. 1, the proposed converter is composed of a voltage regulator and a hig gain boost converter. Voltage regulator is used to regulate the solar panel output and is fed to the high gain boost converter. The high gain boost converter consists of two switches S1 and S2, three diodes D1, D2 and D3, three capacitors C1, C2, C3 and C4, and two inductors L1 and L2 and a small inductor L3 to limit peak current. L3 is chosen very small typically 50 times smaller than L1.

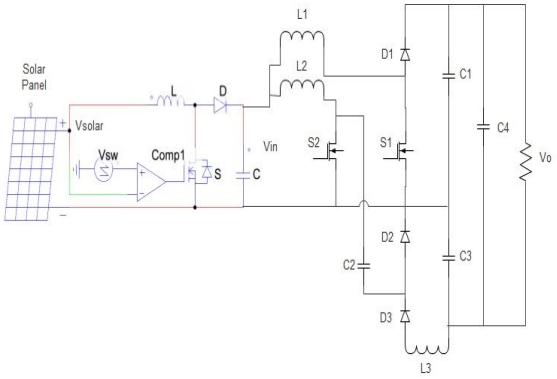

Fig. 1 proposed converter

III. OPERATING PRINCIPLE

In order to illustrate the operation of the proposed converter, several assumptions are made:

1) All switches are ideal.

2) The two inductors L1 and L2are large enough to be consideredas a constant current source during a switching period.

3) The output capacitor $C_4$is large enough to be considered as a constant voltage source of Vin/(D * (1 – D)).

4) All the switches are MOSFETs with parasitic diodes.

The two switches S1 and S2 are complementarily, i.e. when S1 is ONN, S2 is OFF and when S2 is ONN, S1 is OFF. The switching time is Ts, and D is the duty ratio for S2. Therefore S2 is conducting for a period DTs and S1 for (1 – D)Ts.

Mode 1: When the switch S1 is on i.e. during (1 – DTs) period, the equivalent circuit is shown in Fig. 2.Inductor L1 starts charging with negative polarity at diode D1 thus reverse biasing the diode D1 and blocking voltage across capacitor C1. Current through L1 rises with a slope V_{IN}/L1. Also diode D3 is reverse biased blocking voltage across C3. Since the switch S2 is open, L2 forces the diode D2 to turn on. Current through L2 discharges at the rate (V_{IN} - V_{C2})/L2 charging capacitor C2.

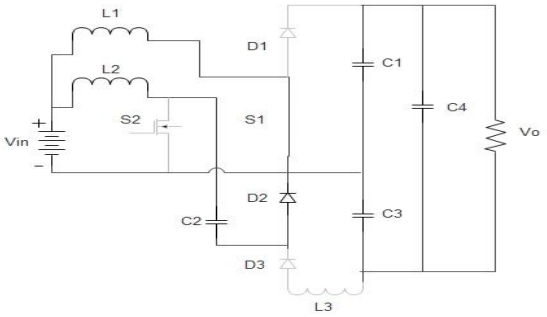

Fig 2. Equivalent circuit when S1 is conducting

*Mode 2:*When S2 is ON (and S1 is OFF) during DTs period, the equivalent circuit is shown in Fig. During this period, L1 forces diode D1 and D3 to turn on. Current through L1 discharges at the rate (V_{IN} - V_{C1})/L1 charging capacitor C1. While S2 is conducting D2 is turned off, inductor L2 stores energy and current through L2 rises with a slope V_{IN}/L2 since S2 is ON.During this period, capacitor C2 and C3 are connected in parallel forming a switched capacitor type circuit. Therefore L3 is used to limit the peak current in the circuit.

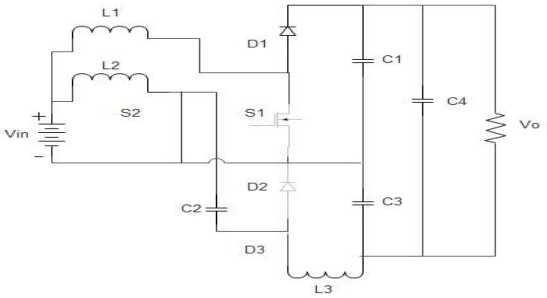

Fig 3. Equivalent circuit when S2 is conducting

Clearly, from the operation of the proposed topology, the input current is sum of currentsthrough L1 and L2. Since L1 and L2 charge and discharge complimentary, the size of the inductors are chosen such that the input current is ripple free at a selected duty cycle.

When the load is connected to the converter, the output voltage also varies with the change in the load. Hence feedback is provided to maintain constant voltage across the load in spite of variation in load.

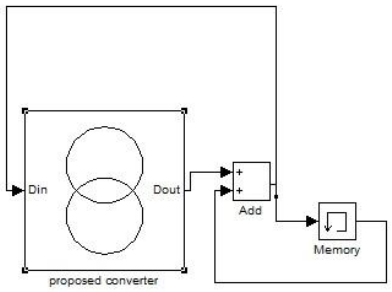

Fig 4. Feedback model of Simulink

The Feedback is given to the Psim model of the proposed converter as shown in fig 5

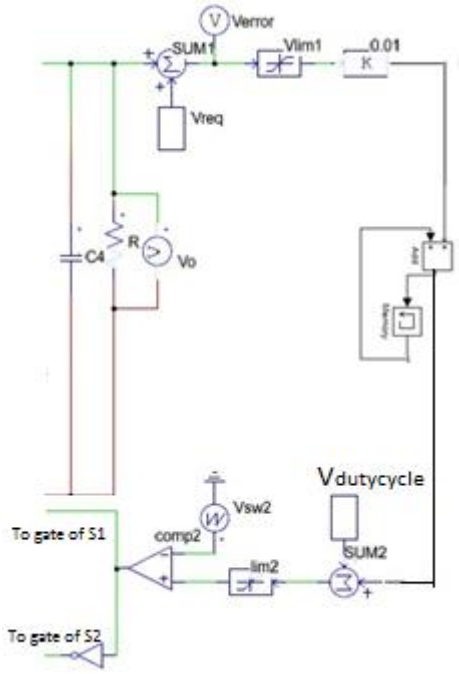

Fig 5. Feedback for the converter

The output voltage from the load is added to the required reference voltage (with gain -1) by using sum block sum1. The error is limited between a maximum and minimum value using limiter, lim1 and is multiplied with gain k. This error value is chosen as outlink node (Dout) from the psim model and is added with the previously stored error value in the memory block by the adder block of the Simulink control loop. The sum value of the adder block is given as inlink node (Din) to the PSIM model. Then, this value from the adder block (in the Simulink control loop) is added with a constant value $V_{Dutycycle}$(which determines duty cycle) by the sum block sum2. The output of sum block 2 is given to the non-inverting terminal of the comparator, comp2 after passing through the limiter, lim2. To the inverting terminal of the comparator a reference saw-tooth voltage is given. Upon comparing the two signals the comparator generates a unity magnitude voltage pulse whenever the input at non-inverting terminal is higher than inverting terminal. This voltage pulse is given to the switch S1 directly through the ON-OFF switch. The output of comp2 is inverted using a NOT gate and is given to switch S2 through the ON-OFF switch.

If the output voltage changes due to change in the load then, the duty cycle is controlled to maintain required constant voltage across the load.

IV. DESIGN CONSIDERATION

The voltage regulator is a simple boost converter, the output voltage for this is given by

$$Vin = \frac{Vsolar}{1 - Dr} \ldots\ldots (1)$$

Vin – output of voltage regulator

Vsolar – input from solar panel

Db – Duty ratio of boost converter

The output of voltage regulator, Vin is given as input to the high gain boost converter.

Since the state variables of L1, L2 and C1 have triangular waveform similar to traditional converters, their dynamics are analyzed by considering their average behavior. While L3, C2 and C3 form an switched capacitor type circuit, hence their dynamics is calculated with additional consideration.

Converter's duty ratio d(t) is defined as percentage of time over the switching period that switch S2 is closed,

$$d(t) = \frac{1}{Ts}\int_{t}^{t+Ts} q2(\tau)d \quad \ldots\ldots\ldots (2)$$

Ts – switching period

q2 switching function - is equal to one when S2 is closed and zero when S2 is open.

Voltage across L1 and L2, neglecting ESR is given by

$$L1\frac{diL1}{dt} = d(vin - vc1) + (1 - d)vin. \ldots (3)$$

$$L2\frac{diL2}{dt} = d(vin) + (1 - d)(vin - vc2) \ldots (4)$$

Under steady state average voltage across inductor is zero.

Equating LHS of (3) and (4) to zero

$$Vc1 = \frac{1}{D}Vin \ldots\ldots (5)$$

$$Vc2 = \frac{1}{(1 - D)}Vin \ldots . (6)$$

Clearly from the above equations, Vc1 and Vc2 are proportional to each other,

$$Vc1 = \frac{1 - D}{D}Vc2 \quad \ldots\ldots (7)$$

$$Vc2 = \frac{D}{(1 - D)}Vc1 \ldots\ldots (8)$$

Current through capacitor C1 is given by

$$C1\frac{dvc1}{dt} = diL1 - (\frac{vc1 + vc3}{R}) \ldots. \ (9)$$

In steady state, average current through capacitor is zero. Equating LHS of 9 to zero, we get

$$IL1 = \frac{1}{D}\left(\frac{vc1 + vc3}{R}\right) \ldots\ldots (10)$$

Since C2 and C3 form an switched capacitor type circuit, therefore average dynamics is not be applied. Average Current through L2 is calculated by considering input-output power balance.

$$IL2 = \frac{1}{(1-D)}\left(\frac{vc1 + vc3}{R}\right) \ldots (11)$$

Since C2 and C3 form an switched capacitor type circuit C2 clamps the voltage across C3, and both feature same voltage.

$$Vc2 = Vc3 \quad \ldots\ldots (12)$$

The output voltage is

$$Vo = Vc1 + Vc3 \quad \ldots\ldots \ (13)$$

Substituting (5), (6) and (12) in (13) we get

$$\frac{Vo}{Vin} = \frac{1}{D(1-D)} \ldots . (14)$$

Substituting (7) and (8) in (10) and (11), IL1 and IL2 can be given by

$$IL1 = (1 + \frac{D}{1-D})\frac{1}{D}\frac{Vc1}{R} = \frac{1}{D(1-D)})\frac{Vc1}{R} \quad (15)$$

$$IL2 = (1 + \frac{1-D}{D})\frac{1}{1-D}\frac{Vc2}{R} = \frac{1}{D(1-D}\frac{Vc2}{R} \ldots\ldots (16)$$

Considering the ESR of L1, inductor L1 voltage is given by

$$L1\frac{diL1}{dt} = d(vin - RL1\ iL1 - vc1) + (1-d)(vin - RL1\ iL1) \ (17)$$

Where RL1 is ESR of L1.Under steady state, the average voltage across inductor is zero.

$$0 = D(Vin - RL1\ iL1 - Vc1) + (1-D)(Vin - RL1\ iL1)$$

$$= Vin - RL1\ iL1 - DVc1 \quad \ldots . (18)$$

Substituting (15) in (18)

$$\frac{Vc1}{Vin} = \frac{1}{D + \frac{RL1}{D(1-D)R}} \ldots\ldots \ (19)$$

Similarly Considering the ESR of L2, inductor L2 voltage is given by

$$L2\frac{2diL1}{dt} = d(vin - RL2\ iL2) + (1-d)(vin - RL2\ iL2 - Vc2) \ldots\ldots (20)$$

Where RL2 is ESR of L2.Under steady state, the average voltage across inductor is zero.

$$0 = D(Vin - RL2\ iL2) + (1-D)(Vin - RL2\ iL2 - Vc2)$$

$$= Vin - RL2\ iL2 - (1-D)Vc2 \quad \ldots\ldots (21)$$

Substituting (16) in (21)

$$\frac{Vc2}{Vin} = \frac{1}{(1-D) + \frac{RL2}{D(1-D)R}} \ldots . (22)$$

Substituting (12), (19) and in (22) in (13)

$$\frac{Vo}{Vin} = \frac{1}{D + \frac{RL1}{D(1-D)R}} + \frac{1}{(1-D) + \frac{RL2}{D(1-D)R}} \ \ldots (23)$$

The voltage gain for various values of duty cycle has been performed and is shown in Fig. 6.

Clearly from the graph, voltage gain is minimum at D=50% and increases as D varies from 50%.

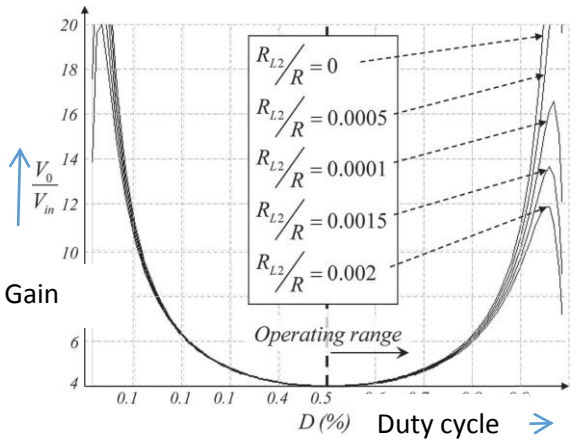

Fig.6 voltage gain vs duty cycle.

1. *Inductor L1 and L2 sizing:*

When S1 is closed i.e. during (1 – D)Ts, voltage across L1 is equal to Vin.

$$VL1 = Vin$$

$$L1\ \frac{diL1}{dt} = Vin$$

$$\frac{\Delta iL1}{\Delta t} = \frac{Vin}{L1}$$

$$\Delta iL1 = \frac{Vin}{L1}(1-D)Ts \quad \ldots . (24)$$

When S2 is closed i.e. during (DTs), voltage across L2 is equal to Vin.

$$VL2 = Vin$$

$$L2\ \frac{diL2}{dt} = Vin$$

$$\frac{\Delta iL2}{\Delta t} = \frac{Vin}{L2}$$

$$\Delta iL2 = \frac{Vin}{L2} D\,Ts \quad \ldots.(25)$$

The input current ripple is the difference between the two inductors current ripple.

$$\Delta i\,in = \frac{Vin}{Fs}\left(\frac{D}{L2} - \frac{(1-D)}{L1}\right) \ldots.(26)$$

The input current ripple can be eliminated by making LHS of (26) to zero, we get

$$L2 = L1\frac{D}{1-D} \ldots..(27)$$

2. Peak current limiting inductor L3 sizing:

When S1 is open, D3 connects C2 and C3 in parallel, hence a inductor is needed to limit the current. The average current through diode is same as load current but shape may be undesirable, hence it has to be controlled.When S2 is closed C2 and C3 are connected in parallel and both will have same voltage. Let this be Vc.0. when S2 is opened for (1 – D)Ts period, they are no longer connected and C3 discharges following the load current and C2 charges following current through L2. Let final voltages across C2 and C3 be Vc2.1 and Vc3.1 can be expressed as

$$Vc2.1 = Vc.0 + Vc2 = Vc.0 + \frac{IL2}{C2}(1-D)Ts \quad (28)$$

$$Vc3.1 = Vc.0 - Vc3 = Vc.0 - \frac{Io}{C3}(1-D)Ts \quad (29)$$

At the end of (1 – D)Ts, the voltage difference between C2 and C3 is given by

$$Vdiff = \Delta vc2 + \Delta vc3 = \left(\frac{IL2}{C2} + \frac{Io}{C3}\right)(1-D)Ts \quad (30)$$

In the absence of peak limiting inductor in series with D3, peak current would be Vdiff over resistance in the loop, on state resistance of S2 and D3 and ESR of C2 and C3. This has been shown in fig. 7 (a)

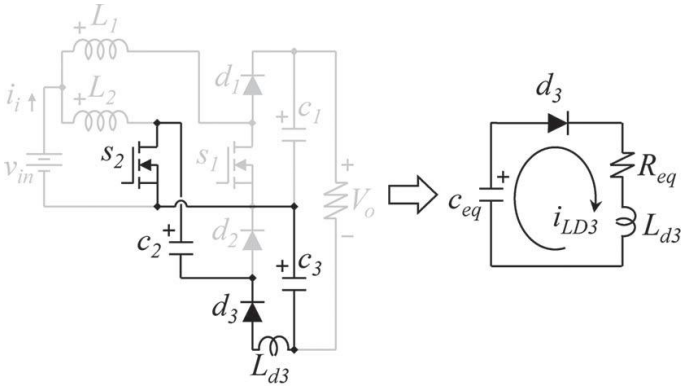

Fig.7(a) equivalent circuit

This may lead to high current that rises above the peak current limit and may destroy the other devices in the circuit. Hence L3 has to be introduced with proper design. Ceq is capacitance of series C2 and C3. Since L3 is very small it charges and discharges completely in a switching cycle limiting the peak current as shown in fig 7 (b).It generates peak resonant at a frequency fo given by

$$fo = \frac{\omega o}{2\pi} = \frac{1}{2\pi\sqrt{(L3Ceq)}} \ldots(31)$$

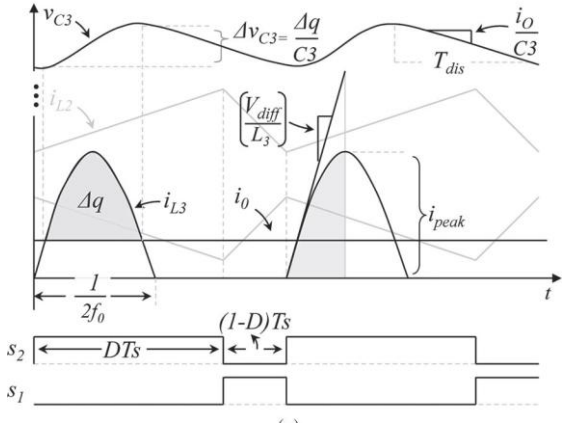

Fig.7 (b) waveform for reactive components

The converter operates at a duty cycle D> 50%, hence L3 should be selected such that fo>Fs.

Fs – switching frequency

The peak current through L3 is given by

$$iL3 = \frac{Vdiff}{\omega o\ Ld3} \ldots.(32)$$

3. Capacitor:

When S1 is closed, current through C1 follows load current, therefore

$$\Delta vc1 = \frac{Io}{C1}(1-D)Ts \quad \ldots.(33)$$

When S1 is closed, C2 charges following current through L2, therefore

$$\Delta Vc2 = \frac{IL2}{C2}(1-D)Ts \quad \ldots.(34)$$

When the current through L3 rises above load current then C3 starts charging with increased voltage $\Delta Vc3$ given by $\Delta q/c3$. The time while C3 is charging is the time when io <iL3(t). C3 discharges through the remaining time of the switching period, therefore

$$Tdis = Ts - (\frac{1}{2fo} - \frac{2}{\omega o}\arcsin\left(\frac{io}{iL3}\right) \ldots(35)$$

Tdis – time in which C3 discharges. During this period, C3 follows load current hence

$$\Delta vc3 = \frac{Io}{C3} Tdis \quad \ldots.(36)$$

V. SIMULATION

ThePsim model of the proposed converter integrated with Matlab Simulink control loop is shown in Fig 8. The simulation of the Model using Matlab 2008 and Psim 9.1 is discussed in this chapter in various sections.

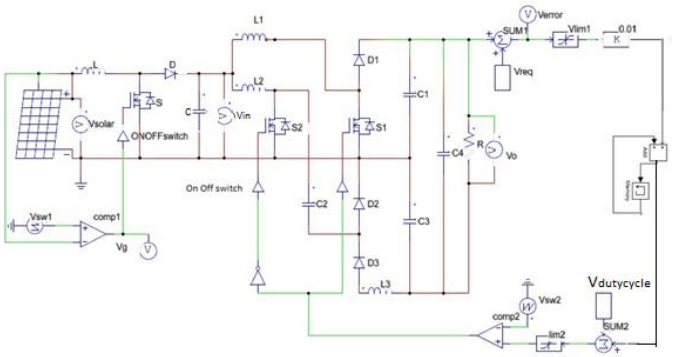

Fig. 8 Psim model of the proposed converter

The converter is simulated for a period of 1 second with the following parameter values.

Parameter	Value
Vsolar	10
L	150 uH
C	220 uF
Vin	16
Duty cycle, D	82.5%
L1	100 uH
L2	470 uH
L3	6 uH
C1, C2 & C3	10 uF
C4	100uF
Fs	25 kHz

The input from solar panel is measured to be 10V. The waveforms for various voltages of voltage regulator are shown in fig 9(a).

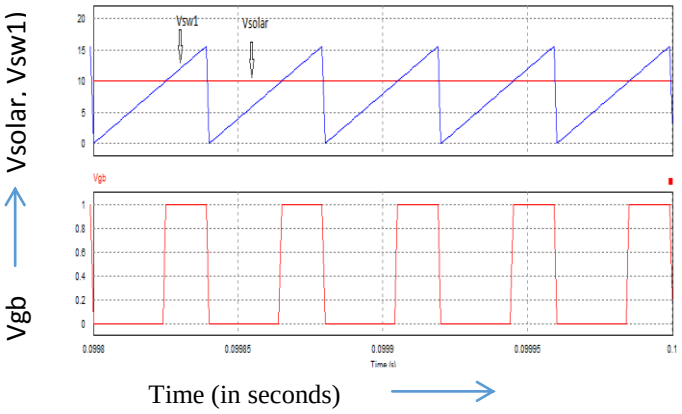

Fig.9(a)Vsolar, sw1 and Vgb

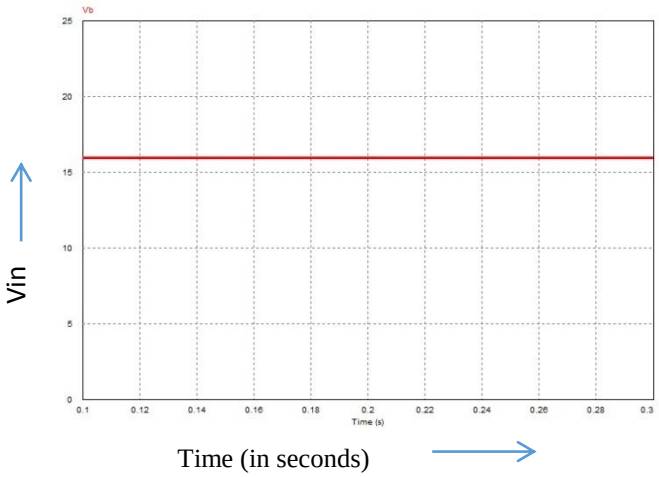

Fig.9(b)Vin

Vs = input voltage from PV cell

Vsw = reference saw-tooth voltage – 15v peak to peak and 25k frequency

Vgb = output of comp1 (voltage pulse to mosfet switch S).

The duty cycle, D is chosen 82.5%, and L1 is selected 100uH, from (27), we get

L2 = 470uH

The peak limiting inductor L3 is very small. Therefore L3 = 6uH is selected.

The output of sum block 2 is given to the non-inverting terminal of the comparator, comp2 after passing through the limiter block, lim2. To the inverting terminal of the comparator a reference saw-tooth voltage is given. The Comp2 generates a unity magnitude voltage pulse whenever the input at non-inverting terminal is higher than inverting terminal. This voltage pulse is given to the switch S1 directly through the ON-OFF switch. The output of comp2 is inverted using a NOT gate and is given to switch S2 through the ON-OFF switch. This is shown in Fig. 10

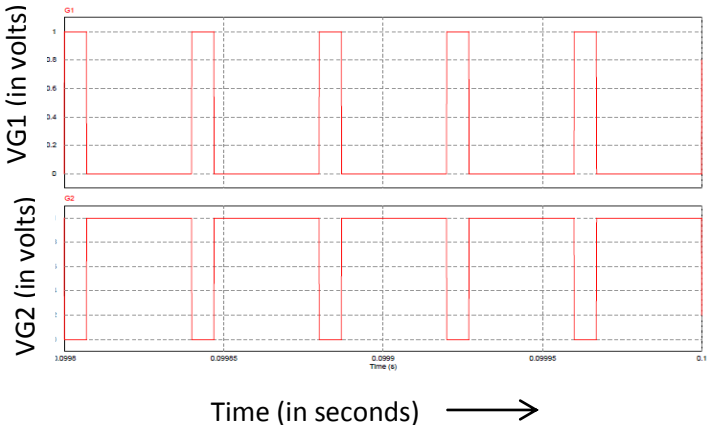

Fig.10 pulse signals to MOSFET switches

The input current corresponds to the sum of current through L1 and L2. The inductors are selected such that both inductors are charged with same voltage. Since L1 and L2 charge/discharge in a complementary manner, the input current is ripple free as shown in Fig. 11. A small inductor L3 is used to limit the peak current when C2 and C3 are connected in parallel.

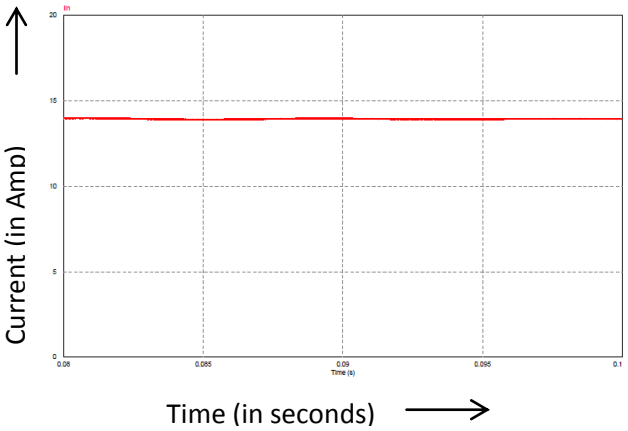

Fig.11 input current

When S1 is closed Current through L1 rises with a slope $V_{IN}/L1$ hence diode D1 and D3 are reverse biased, while S1 is conducting D2 is forward biased and Current through L2 discharges at a rate of $(V_{IN} - V_{C2})/L2$ charging capacitor C2.

On the other hand, when S2 is closed Current through L2 rises with a slope $V_{IN}/L2$, reverse biasing D2. While S2 is conducting, current through L1 discharges at a rate $(V_{IN} - V_{C1})/L1$ through D1 charging the capacitor C1. Furthermore D3 is forward biased and hence C2 and C3 are connected in parallel. Current through L1 and L2 is shown in Fig. 12.

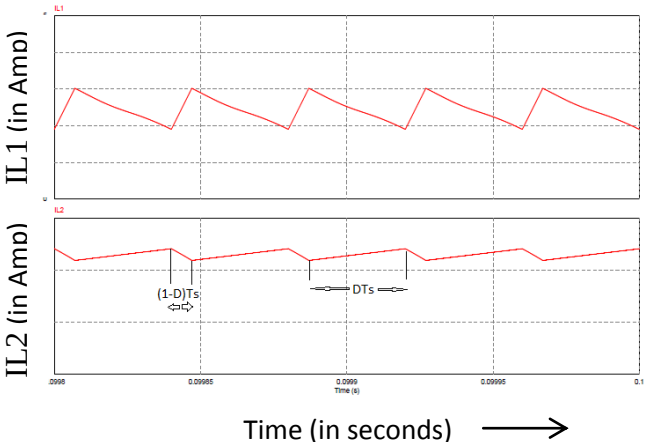

Fig.12 currentthroughinductors

When S1 is closed, diode D1 is reverse biased blocking the voltage across C1 and diode D3 is reverse biased blocking the voltage across C3 while L2 discharges charging the capacitor C2. On the other hand When S2 is closed, L1 discharges through D1 charging capacitor C1 and D2 is reverse biased. Furthermore while S2 is conducting D3 is conducts and therefore C2 and C3 are connected in parallel forming a switched capacitor type behaviour. The voltage across capacitor C1 and C2 is shown in Fig. 13.

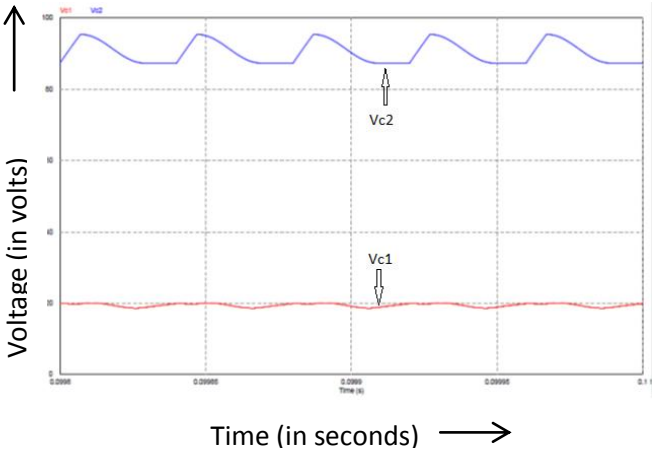

Fig.13 Voltage across capacitors

The output voltage Vo given by (26) is sum of voltage across C1 and C3, is shown in Fig. 14. Vo is measured to be 110V.

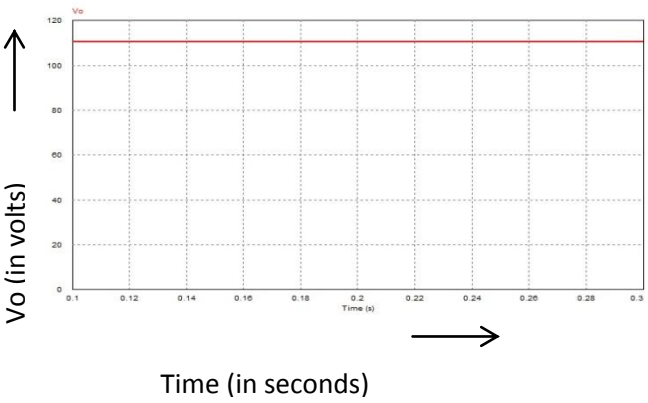

Fig.14 Output voltage

An output capacitor C4 = 100 uF is used to remove the ripples from the output voltage.

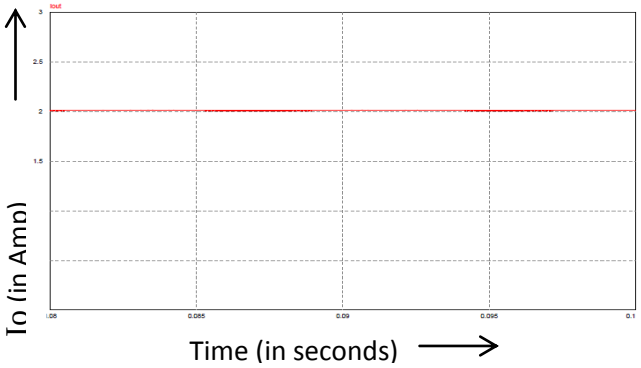

Fig.15 load current

A resistive load R = 55 Ω is connected across capacitor C4. Current drawn by the load is shown in Fig. 15

With the feedback, R can be varied between 5 to 550. If the output voltage falls or rises above the required reference value then the duty cycle is controlled using the feedback to the converter so that output voltage remains constant at 110V.

APPLICATIONS

- Used in street LED lightening, 40-100V.
- Used in SMPS power supplies for Desktop, LED TV, LCD displays.
- Used in Industrial control and Process control instrument set up.

VI. CONCLUSION

The proposed converter uses solar energy as input and achieves a high voltage gain without utilizing extreme duty cycle. Also the converter is able to remove the input current ripple at a preselected duty cycle. Furthermore with the feedback, the converter is able to maintain constant output voltage if the output voltage changes due to change in the load i.e. load regulation. Also in this converter, smaller reactive components are used which has more advantages compared to the use of transformers.

The converter is able to achieve zero ripples in the input current at a preselected duty cycle; it can be improved by designing optimal size of the inductors for a wide range of duty cycle.

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