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# Triangular Gate-all-around Nanowire FETs with Enhanced Electrical Performance using High-K Dielectric Gate Oxide

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***Abstract*—In this paper the enhanced electrical performance of Triangular Gate-all-around Nanowire FETs has been reported using High-K dielectric gate oxide for 14 nm gate length. It was found that by using High-K dielectric material like Hafnium (IV) oxide instead of using Silicon Dioxide the electrical performance improved significantly. ON-OFF Current ratio improved by 184.99 %, Drain Induced Barrier Lowering reduced by 33.33 %, Sub threshold Swing reduced by 1.53%, Off state leakage current reduced by 18.50% and on current increased by 132.26%. 3D Technology Computer-aided Design numerical simulator was used to perform all device simulation using Drift Diffusion approach with Density Gradient Quantum Corrections model.**

***Keywords*— *Gate all around, FET, High-K dielectric and Numerical Simulation.***

## I. INTRODUCTION

In this last decade, due to continuous downscaling of silicon MOSFETs the short channel effects (SCE) has become a major concern in order to meet the International Technology Roadmap of Semiconductors (ITRS) projections [1-4]. In this context, Gate-all-around (GAA) Nanowire FETs are consider as a promising transistor structure, which enables further gate length scaling beyond 22 nm because of its superior SCEs immunity realized by all around gate structure [5-6].

The insulator layer in the field effect transistors system electrically separates the different semiconductor region like source, drain and channel from the gate electrode, while simultaneously serving as a medium transferring the field effect of the gate electrode in the semiconductor region. The thinner the insulator layer, the higher the electron concentration induced at the semiconductor surface. Additionally, thinning the insulator layer shields the channel carriers from the fringing field lines originated in the drain, thereby reducing SCEs. Thus, the SCEs of GAA Nanowire FETs can be further reduced by scaling down the gate oxide layer. However, scaling of silicon based oxide below 2 nm results in an increase of gate tunnel leakage current [3]. Intel in 2007 introduced Hafnium-based oxides as a replacement for silicon oxide as a gate insulator in MOSFETs in 45nm technology [7]. In the previous reported work the use of dielectrics with high permittivity (high-k dielectrics) instead of silicon dioxide has shown the further scaling of gate oxide with performance improved of conventional MOSFETs and FinFETs [8-10].

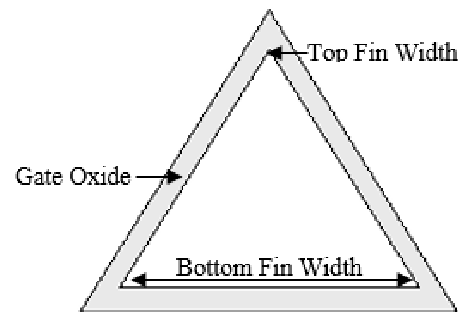


Fig. 1 Systematic diagram of Fin cross section view of Triangular GAA Nanowire FETs

In this paper the comparative electrical performance analysis of Triangular GAA Nanowire FETs with High-K Dielectrics material Hafnium (IV) oxide ($HfO_2$) and Silicon Dioxide ($SiO_2$) has been done in terms ON current, OFF current, Drain Induced Barrier Lowering and Sub Threshold Swing for 14 nm gate length. The systematic diagram of fin cross section has been shown in the Fig. 1. This paper has been presented in the following manner Section 2 describes the device design and simulation approach. Section 3 shows the results and discussions of the proposed work. Subsequent Section concluded the work.

## II. DEVICE DESIGN AND METHODOLOGY

Triangular GAA Nanowire FETs structures was designed by using Cogenda GDs2mesh 3D Technology Computer-aided Design numerical simulator (TCAD) model construction tool [11]. Triangular Fin of GAA Nanowire FETs was designed with the bottom fin width ($W_{fin, bot}$) of 10 nm and top fin width ($W_{fin, top}$) of ~ 0 nm. Non-vertical sidewalls was taken symmetric with equal swings of the lateral sides. The nominal device parameters have listed in Table I. The 3D illustrations of the designed Triangular GAA Nanowire FETs devices is shown in Fig. 2. Fig.2 (a) show the active region fin of the device which of triangular shape. Fig.2 (b) show the source pad, drain pad, active region that was etched on substrate. The active region was etched at height of 30 nm above the substrate this 30 nm represent the shallow trench isolation of the device. Tungsten with work function 4.50eV was used for metal gate.



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TABLE I. DEVICE PARAMETERS

| Parameter | Value |
|---|---|
| Gate Length | 14 nm |
| Fin Height | 30 nm |
| Gate Oxide Thickness | 1 nm |
| Top Fin Width | ~ 0 nm |
| Bottom Fin Width | 10 nm |
| Source/Drain Doping(donor) | $1\times10^{20}$ $cm^{-3}$ |
| Substrate Doping (acceptor) | $1\times10^{17}$ $cm^{-3}$ |

Fig. 2 (c) shows the metal gate and metallic contact aluminum that was used for power supply. Finally, to separate different region from each other the silicon dioxide was formed as shown in the Fig. 2 (d). Similarly for the second device Hafnium (IV) oxide was formed to separate different region from each other as shown in the Fig. 2 (e) keeping all other parameters and process same as that of Triangular GAA Nanowire FETs with Silicon Dioxide dielectric. Fig. 2 (f) shows the color index for different material. Lightly doped silicon channels are used to reduce random dopant fluctuation and to eliminate the threshold voltage and mobility variability [4]. For substrate the doping concentration is 1e17 $cm^{-3}$ of acceptor type and is doped uniformly. For source/drain the doping concentration is 1e20 $cm^{-3}$ of donor type and the doping profile is Gaussian.

Triangular GAA Nanowire FETs devices has been simulated using Cogenda Visual TCAD numerical simulator. The carrier transport was defined using classical drift diffusion (D-D) approach with density gradient approach based quantum corrections [12]. In order to characterize the electrical performance of GAA FETs accurately, it is important to consider quantum confinement effects. The most acceptable choice for the inclusion of quantum corrections in D-D simulations is the density gradient approach [13].The Carrier transport is defined using D-D model which mainly uses Poisson's equation can be expressed as follows:

$$\nabla.\varepsilon\nabla\varphi = -q(p - n + N_D^+ - N_A^-) \quad (1)$$

For inclusion of Quantum confinement effects can be included in D-D model by including the quantum potential in calculating the driving force of electrons and holes. This correction term is related to the density gradient of carrier concentration [13-15].

$$\Lambda_n = -a_n \frac{\nabla^2\sqrt{n}}{\sqrt{n}} \quad (2)$$

$$\Lambda_p = a_p \frac{\nabla^2\sqrt{p}}{\sqrt{p}} \quad (3)$$

Where $\varphi$ is the electrostatic potential of the vacuum, n and p are the electron and hole concentration respectively, $N_D^+$ and $N_A^-$ are concentration of donor and acceptor ions respectively and $q$ is electron charge. $a_n = \frac{\hbar^2\gamma n}{6qm_n}$ and $a_p = \frac{\hbar^2\gamma p}{6qm_p}$ are the coefficients with $m_n$ and $m_p$ being the electron and hole effective masses respectively.

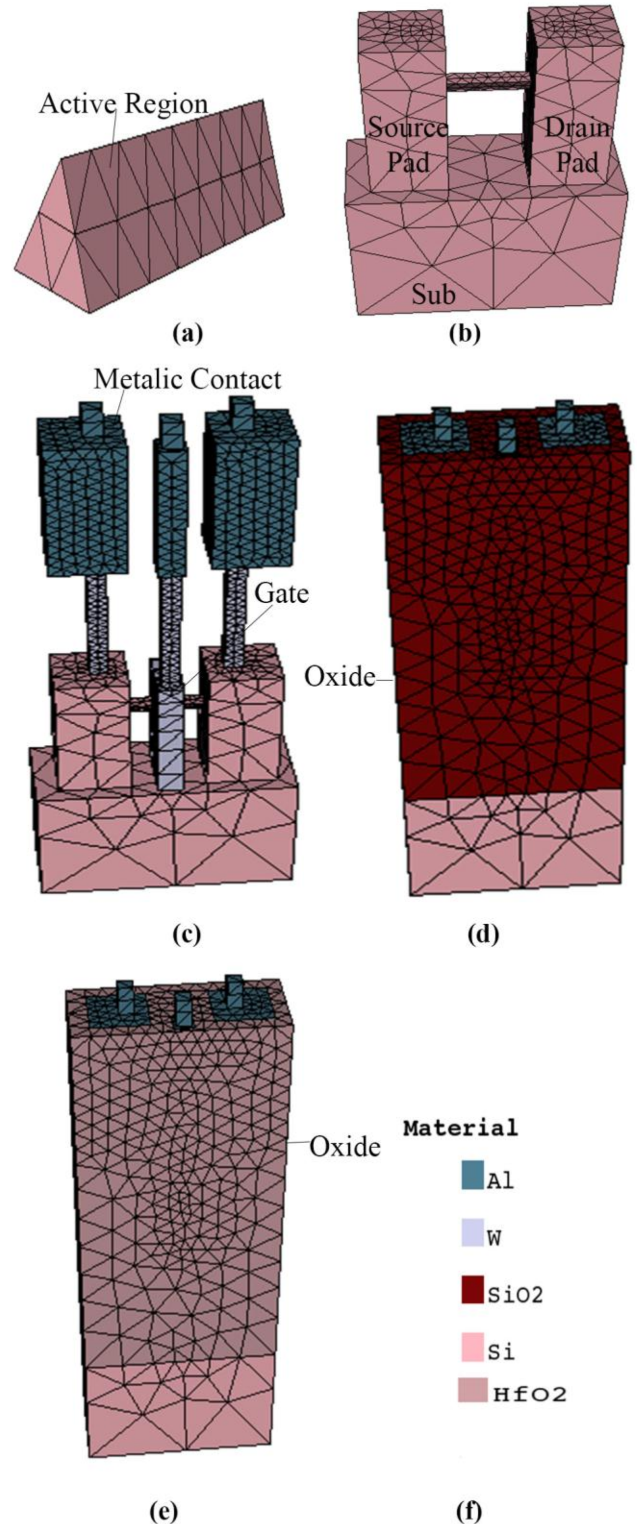


Fig. 2 Bird's eye view of Triangular GAA Nanowire FETs illustrations; (a) Triangular Fin shape active region, (b) Active region with source and drain pad, (c) Formation of metallic gate and power supply contact, (d) Formation of silicon dioxide to separate each layers, (e) Formation of Hafnium (IV) oxide to separate each layers and (f) color index for different material.



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## III. RESULT AND DISCUSSION

The threshold voltage was calculated using maximum Trans conductance change method for both Triangular GAA Nanowire FETs directly from its V-I characteristics with drain voltage of 50 mV [16].

The on-current was measured at gate voltage, $V_g$ = 1V and off-current at $V_g$ = 0V in the linear region with drain voltage of 50 mV. The sub threshold swing is the change in the gate voltage per decade change in drain current.

$$SS = dV_g / dlog(I_d) \qquad (4)$$

The DIBL parameter is the horizontal displacement of the transfer characteristics at constant drain current ($I_{cd}$) for drain voltage $V_g$= 0.02 and 1V [17].

$$I_{cd} = (W_{eff}/L_g) \times 10^{-7} \qquad (5)$$

The effective channel width, ($W_{eff}$ ) for Triangular GAA Nanowire FETs is define as

$$W_{eff} = 2W_{fin,eq} + 2H_{fin} \qquad (6)$$

The fin width ($W_{fin}$) for Triangular GAA Nanowire FETs varies in the range of top fin width ($W_{fin,top}$) and bottom fin width($W_{fin,bot}$). The equivalent fin width $W_{fin,eq}$ of Triangular GAA Nanowire FETs can be given at its orthocenter [17].

$$W_{fin,eq} = W_{fin,top} + \frac{\beta}{\beta + 1}(W_{fin,bot} - W_{fin,top}) \qquad (7)$$

$$\beta = \frac{2W_{fin,bot} + W_{fin,top}}{2W_{fin,top} + W_{fin,bot}} \qquad (8)$$

The simulated V-I characteristics of Triangular GAA Nanowire FETs with silicon dioxide dielectric and with Hafnium (IV) oxide dielectric have been shown in the Fig. 3 and Fig. 4 respectively. The transfer characteristics has been plotted for drain voltage of 50 mV and 1V in linear as well as logarithmic scale and the output characteristics for different gate voltage ranging from 0.6 to 1.2V. The calculated electrical parameter value of both Triangular GAA Nanowire FETs have been listed in the Table II. By replace the silicon dioxide dielectric with high-k dielectrics Hafnium (IV) oxide of Triangular GAA Nanowire FETs the off state leakage current reduced by 18.50%, on current increased by 132.26%, $I_{ON}/I_{OFF}$ ratio improved by 184.99 %, DIBL reduced by 28.20 % and SS reduced by 1.53%. The threshold voltage was almost same for both Triangular GAA Nanowire FETs because of the lightly doped channel. The transfer characteristics comparison of Triangular GAA Nanowire FETs with silicon dioxide and Hafnium (IV) oxide for drain constant voltage of 50mV is shown in the Fig. 5.

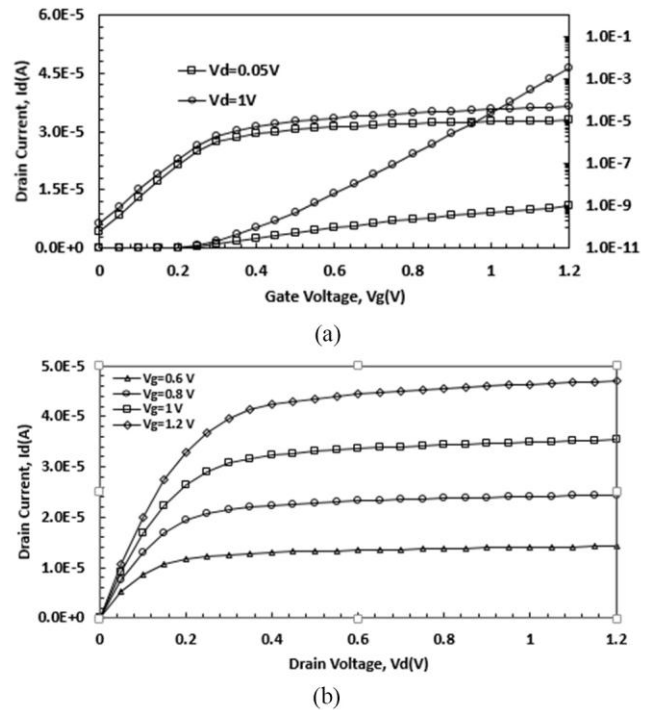


Fig. 3 Simulated V-I characteristics (a) Transfer characteristics in linear and logarithmic scales and (b) Output characteristics of Triangular GAA Nanowire FETs with silicon dioxide as dielectric.

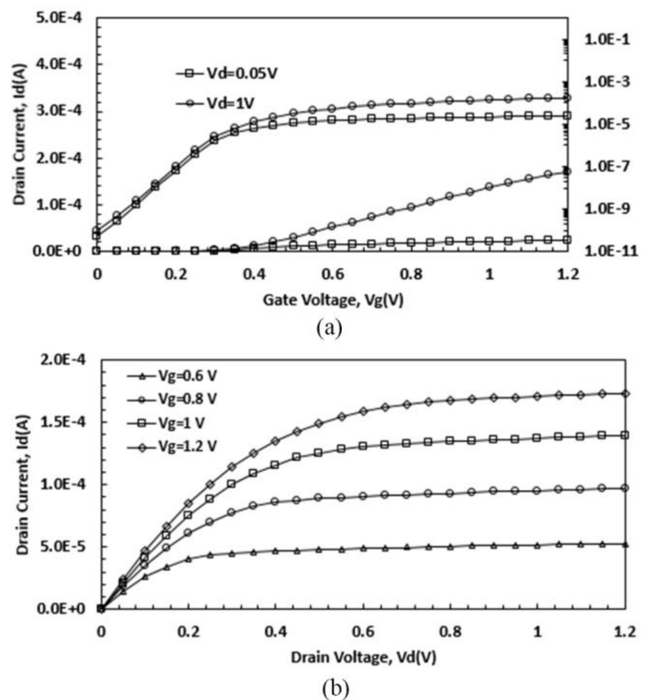


Fig. 4 Simulated V-I characteristics (a) Transfer characteristics in linear and logarithmic scales and (b) Output characteristics of Triangular GAA Nanowire FETs with Hafnium (IV) oxide as dielectric.



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TABLE II. ELECTRICAL PARAMETERS OF SIMULATED TRIANGULAR GAA NANOWIRE FETS.

| Parameter | Triangular GAA Nanowire FETs ($SiO_2$) | Triangular GAA Nanowire FETs ($HfO_2$) |
|---|---|---|
| $V_T$ (V) | 0.241 | 0.245 |
| $I_{ON}$ (A) | 9.21E-06 | 2.14E-05 |
| $I_{OFF}$ (A) | 6.02E-11 | 4.91E-11 |
| $I_{ON}/I_{OFF}$ | 1.53E+05 | 4.36E+05 |
| DIBL (mV/V) | 48 | 32 |
| SS (mV/dec) | 65 | 64 |

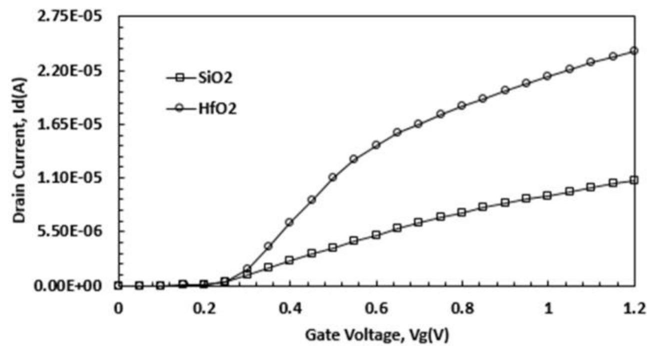


Fig. 5. Comparison of simulated transfer characteristics of Triangular GAA Nanowire FETs with Hafnium (IV) oxide and silicon dioxide as dielectric for $V_d$ = 0.05 V.

The above simulation results of Triangular GAA Nanowire FETs have shown that high-k dielectrics Hafnium (IV) Oxide can improve the device performance and also it can be used to further scale down the gate oxide below 2nm. This improved in electrical performance is due to high dielectric constant of $HfO_2$ which is 4–6 times higher than that of $SiO_2$.

## IV. CONCLUSION

The electrical performance analysis of Triangular GAA Nanowire FETs with silicon dioxide and Hafnium (IV) oxide for 14 nm gate length have shown that the high-k dielectrics Hafnium (IV) oxide can improve the devices performance of GAA Triangular FETs. This improvement is due to high dielectric constant of Hafnium (IV) oxide. Gate oxide thickness can be further scale down below 2nm using High k dielectric material like Hafnium (IV) oxide. The scaling down of gate oxide thickness improve gate controllability of channel and hence reduction in short channel effects.

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