VLSI Architecture For Area And Power Optimized Spectrally Efficient FDM Transmitter

[1] Nivedita. J, [2] Venkatesan. K
[1]PG Scholar, Department of Electronics and Communication Engineering, Sri Shakthi Institute of Engineering and Technology, Coimbatore
[2]Assist. Prof. ECE, Sri Shakthi Institute of Engineering and Technology, Coimbatore

Abstract

Spectrally Efficient FDM employs non-orthogonal overlapped carriers to improve spectral efficiency for future communication systems. Non-orthogonal multicarrier systems achieve spectral savings by either reducing the spacing between the subcarriers in frequency or transmission time. But the loss of orthogonality complicates both signal generation and detection. SEFDM signal shall be realized with standard IDFT blocks judiciously arranged for SEFDM modulation. A VLSI architecture based on multistream FFT, which offers substantially reduced circuit area and power is used this work.

Keywords—Bandwidth efficiency, multicarrier modulation, transmitter, wireless communications.

1. Introduction

The ever growing demand from the wireless communications has always inspired the research for techniques to save the spectrum and combat wireless channel impairments. Spectrally efficient frequency division multiplexing (SEFDM) system promises better utilization of bandwidth by reducing the spacing of sub-channels. The first systems to appear were Fast OFDM (FOFDM) [1] and m-ary amplitude shift keying OFDM (MASK) [2], both of which halve the spectrum utilization, but are constrained to one dimensional modulations such as BPSK and M-ary ASK. All variants of SEFDM systems are basically multicarrier modulation schemes that multiplex non-orthogonal overlapped sub-carriers. Following this, came spectrally efficient FDM (SEFDM) [3], high compaction multicarrier-communications (HC-MCM) [4], overlapped FDM (Ov-OFDM) [5] and multi-stream faster than Nyquist signalling (FTN) [6]–[8] all of which promote variable spectral utilization savings for two dimensional modulations. In principle, non-orthogonal multicarrier systems achieve spectral savings by either reducing the spacing between the subcarriers in frequency and/or transmission time, thus, communicating information at a faster than Nyquist rate.

Despite the favourable spectral savings on offer, in practice, the loss of orthogonality complicates both signal generation and detection. For the detection, Maximum likelihood (ML) is suggested as the optimum technique in additive white Gaussian noise (AWGN) channels[1]. Nevertheless, ML detection is overly complex, with a computational complexity that grows exponentially with the size of the system.

As for the generation of SEFDM modulated symbols, the SEFDM signal can be realized with a similar complexity to OFDM system[14], by utilizing standard inverse discrete Fourier transform (IDFT) blocks, judiciously arranged for SEFDM modulation. Minor modifications on the input streams are needed and the designs rely mainly on standard IDFT operations that can be efficiently realized with the inverse fast Fourier transform (IFFT) algorithm.

In this paper, we introduce a VLSI architecture based on the FFT, which offers substantially reduced complexity analysis. The FPGA implementation is intended for use in an SEFDM performance evaluation test bed to further enable practical demonstration of the spectrally efficient physical layer.

2. The SEFDM System

SEFDM signal is constructed by modulating a block of the input data stream on parallel carriers, as shown in Fig1. The carriers in FDM systems are spaced by a fraction of the inverse of the symbol duration, violating orthogonality condition of OFDM systems where the spacing is inversely proportional to the symbol duration. The distance between the carriers in frequency, denoted by Δf is given by $\Delta f = \alpha/T$ where α is BW compression and T is duration of one SEFDM symbol. SEFDM signal is generated using a bank of modulators that generates the sub carriers. It requires high frequency precision in order to reduce frequency offset effects. Each of the N complex input symbols modulates one of the non-orthogonal and overlapping subcarriers, hence, giving the SEFDM signal x (t) as

$$X(t)=\frac{1}{\sqrt{T}}\sum_{l=-\infty}^{\infty}\sum_{n=0}^{N-1} s_{l,n}\, e^{\left(\frac{j2\pi n\alpha(t-lT)}{T}\right)} \qquad (1)$$

The preceding analysis in AWGN channels is included here as a general introduction to SEFDM system performance. Notwithstanding, the effects of frequency selective fading are of key significance and transmission over different fading channel conditions is an important area of study for wireless systems.

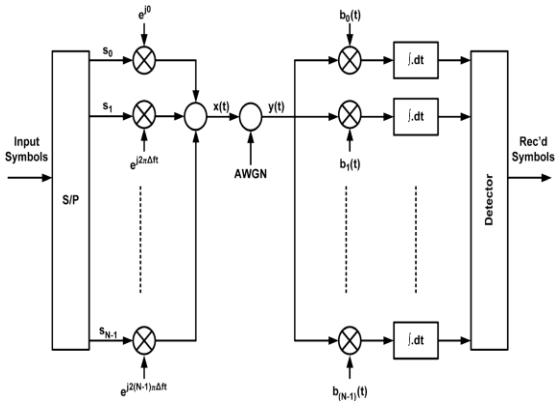

Fig.1 SEFDM block diagram

3. The IDFT Design of SEFDM Signals

3.1 General Description

In analogy to OFDM, it is shown that the SEFDM signal can be expressed by IDFT operations. It is shown that there are ways to express the SEFDM signal with an IDFT operation with simple manipulations of the input symbol vectors. These manipulations are merely in the form of zero insertions either at the end of the vector only, in a manner similar to zero padding and/or between the symbols. The change in length ensures the alignment of the IDFT frequency samples and the SEFDM subcarriers and the zeros suppress the unwanted frequencies.

The samples of the SEFDM signal can be generated using c IDFT operations each of length of N points. The input symbols are padded with (c-1) N zeros and then arranged as a $c \times N$ matrix in column major order. An IDFT operation is then performed on each row. The signal is finally composed by combining rotated versions of the IDFT outputs as depicted in Fig3.

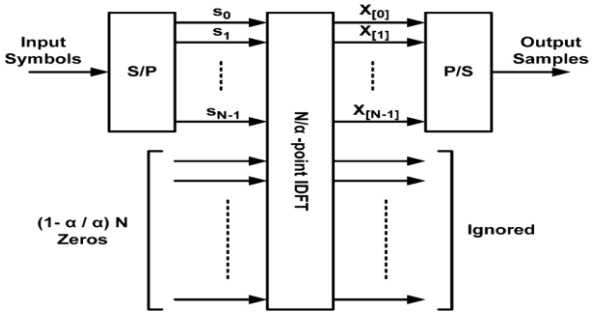

Fig.2 Generating SEFDM signal based on a single IDFT operation

For integer values of N/ α (i.e., $(N/\alpha)\in \mathbb{Z}$), the work in shows that a discrete SEFDM signal X (k) can be described as

$$X|k| = \acute{X}|k|, \text{ for k=1...N-1} \qquad (2)$$

Where

$$\dot{X}(k) = F^{\frac{N}{\alpha}}\{\acute{S}\}$$

and $F^{\frac{N}{\alpha}}\{.\}$ is the N/ α point IDFT of the argument, with $\acute{S}$ being a vector of length N/ α, whose elements $\acute{s}_i$ take the values of either input symbols s_i or zeros as

$$\acute{S}=\begin{cases} S_i, 0 < i < N \\ 0, N \leq i < \mathrm{N}/\alpha \end{cases} \quad (3)$$

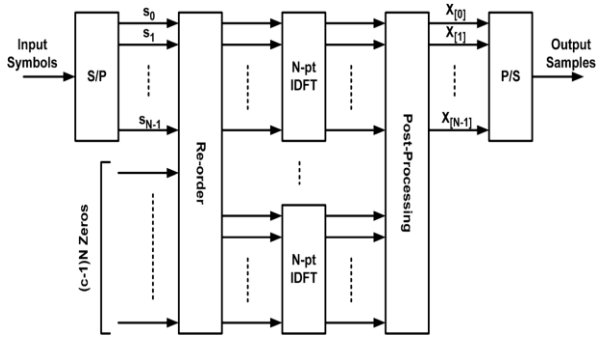

Fig.3 SEFDM IDFT-based transmitter with multiple IDFT operations

Thus the SEFDM signal can be realized with a single IDFT block, with a length longer than N. The SEFDM transmitter in this case depicted in Fig2. Furthermore, it is shown in that by expressing the term α as a rational number, that is by taking$\alpha = b/c$, where both b and c are integers and b<c, the SEFDM signal can be expressed as

$$\mathrm{X}(k) = \frac{1}{\sqrt{N}} \sum_{n=0}^{cN-1} \acute{s}_n e^{\frac{j2\pi nkb}{cN}} \quad (4)$$

As for the case above, here we define $\acute{S}$ to be a vector of length cN whose element $\acute{s}_i$ take the values of either the input symbols $s_{i/b}$ or zeros as

$$\acute{S}=\begin{cases} S_{i/b}, & i \in I \\ 0, otherwise \end{cases} \quad (5)$$

and I = {0,b,...,b(N-1)}. The equation (10) can be rearranged as,

$$\mathrm{X}(k)=\frac{1}{\sqrt{N}} \sum_{i=0}^{c-1} e^{\frac{j2\pi nkb}{cN}} \sum_{m=0}^{N-1} \acute{s}_{i+mc} e^{\frac{j2\pi nkb}{cN}} \quad (6)$$

By substituting with n=$i + mc$.

4. VLSI Architecture

4.1 SEFDM Transmitter

The SEFDM signal is composed of a combination of symbols each modulated on one of the subcarriers. Therefore, the conventional SEFDM transmitter consists of a bank of modulators running at the subcarriers frequencies as can be seen in Fig3

4.1.1 Zero Insertion and Reorder

Fig4 illustrates the general symbol reordering operation, which consists of padding the input symbols with (c-1)N zeros before arranging them as a $c \times$ N matrix in column major order. A implementation of this operation implies a buffer of complex words to hold the sparse complex matrix. However, since each incoming symbol is mapped to only one IFFT input, it is only necessary to use a multiplexer in front of each IFFT to choose either the incoming s_i symbol or 0+ j0 samples.

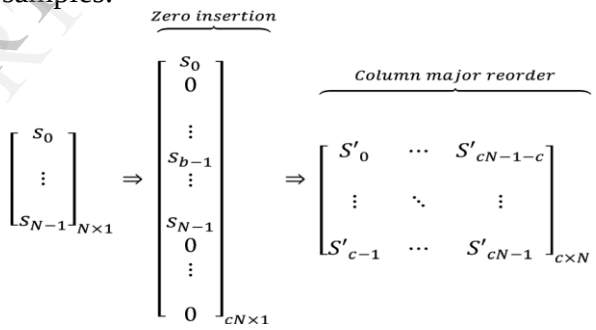

Fig.4 General Operation of symbol reordering

4.1.2 Parallel IFFTs

The N -point IDFTs are implemented in this section as cN -point IFFTs, which can be implemented as c parallel IFFT blocks. Using c parallel IFFTs allows the highest throughput and constant latency independent of , at the cost of linear increase in area and power. Here used 16-point, 8-bit complex IFFT blocks-based on radix-2^2 flow graph. The IFFTs have an enable signal which when de-asserted gates the internal clock and clears the output registers to zero.

4.1.3 Postprocessing

The post processing operation combines the parallel IFFT outputs after multiplication with a complex exponential in order to produce the discrete-time output samples, X|k.| The complexity of the post processing is linear functions of c, where we require (c-1) complex multiply accumulate (CMAC) operations. The hardware required includes the CMACs and LUTs to store precalculated rotation coefficients in read-only memory (ROM).

4.2 Whole Trellis Stage Pruning for α≤ 1/2

In this case, the reordered zero bins Fig.4 are arranged in a compact manner such that nonzero bins are followed by at least $N/2$ contiguous zeros. Hence, the first IFFT trellis stage contains only half BFs and can be pruned entirely up to the input to the first complex multiplier, removing $c.(N/2)$ BF operations and $c.(N/2)$ complex words of storage. Fig6 shows the IFFT signal flow graph for $\alpha = 1/2$, showing the gray edges which are redundant. Unfortunately, as previously mentioned, bandwidth compression ratios less than 1/2 incur a BER penalty and hence this optimization is only really applicable to $\alpha = 1/2$, at least in this particular application.

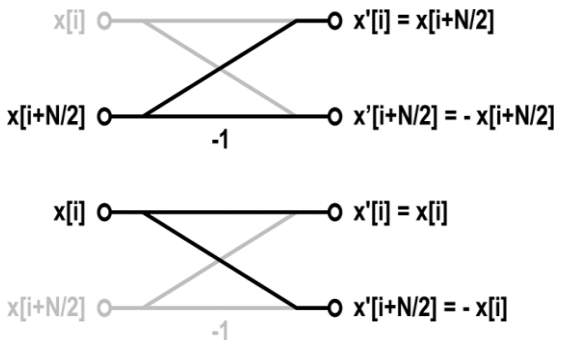

Fig.5 Partially pruned half BFs occur when one of the complex inputs is zero

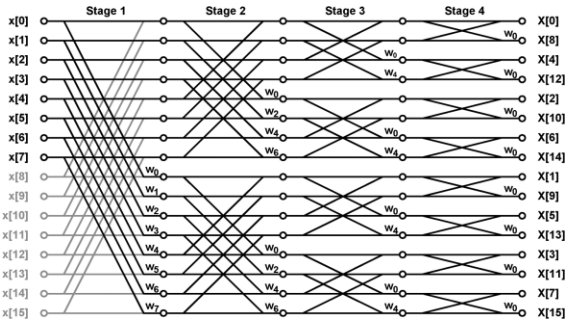

Fig.6 IFFT signal flow graph for $\alpha = 1/2$, N=16

5. Implementation Results

The proposed architecture has been implemented in VHDL and verified using ModelSim simulator. IDFT core was generated by the Xilinx LogiCORE™ IP inorder to optimize this block and also the clock period of 4ns was achieved. The results are shown below.

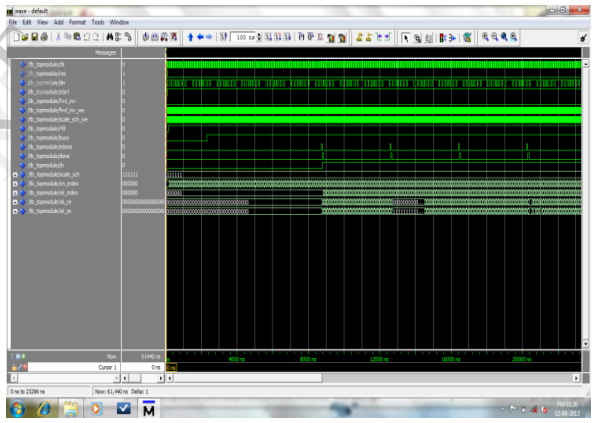

Fig.9 Output of SEFDM Transmitter

6. Conclusion

The newly developed SEFDM system is described. These results demonstrate that a reconfigurable SEFDM transmitter can be realistically implemented with a modest increase in circuit area and power dissipation when compared to conventional OFDM.

References

[1] M. R.D. Rodrigues and I.Darwazeh, "Fast OFDM:A proposal for doubling the data rate of OFDM schemes," *in Proc. Int. Conf. Telecomm.*, Jun. 2002, vol. 3, pp. 484–487.

[2] F. Xiong, "M-ary amplitude shift keying OFDM system," *IEEE Trans. Commun.*, vol. 51, no. 10, pp. 1638–1642, Oct. 2003.
[3] M. R. D. Rodrigues and I. Darwazeh, "A spectrally efficient frequency division multiplexing based communications system," *in Proc. 8th Int. OFDM Workshop*, Hamburg, Germany, 2003, pp. 48–49.
[4] D. Dasalukunte, F. Rusek, and V. Owall, "Multicarrier faster-than- Nyquist transceivers: Hardware architecture and performance analysis," IEEE Trans. Circuits and Systems I: Regular Papers, vol. 58, no. 4, pp. 827–838, Apr. 2011.
[5] J. Mazo, "Faster than Nyquist signalling," *Bell Syst. Tech.* J., vol. 54, pp. 429–458, Oct. 1975.
[6] I. Kanaras, "Spectrally efficient multicarrier communication systems: Signal detection,mathematicalmodelling and optimisation," Ph.D. dissertation, Dept. of Electron. and Elect. Eng., Univ. College London, London, U.K., 2010.
[7] R. Grammenos, S. Isam, and I. Darwazeh**,** "FPGA design of a truncated SVD based receiver for the detection of SEFDM signals," *in Proc. IEEE 22nd Personal, Indoor, Mobile Radio Commun. Symp.*, 2011, pp. 2085–2090.
[8] I. Kanaras, A. Chorti, M. Rodrigues, and I. Darwazeh, "Spectrally efficient FDM signals: Bandwidth gain at the expense of receiver complexity," in *Proc. Int. Conf. Commun.*, 2009, pp. 1–6.
[9] S. Isam, I. Kanaras, and I. Darwazeh, "A truncated SVD approach for fixed complexity spectrally efficient FDM receivers," in *Proc. IEEE Wireless Commun. Netwo. Conf.*, 2011, pp. 1584–1589.
[10] S. Isamand I. Darwazeh, "Design and performance assessment of fixed complexity spectrally efficient FDM receivers," in *Proc. IEEE 73rd Veh. Technol. Conf.*, 2011, pp. 1–5.
[11] S. Ahmed and I. Darwazeh, "IDFT based transmitters for spectrally efficient FDM system," in *Proc. London Commun. Symp.*, Sep. 2009 [Online]. Available:http://www.ee.ucl.ac.uk/lcs/previous/ LCS2009/index.html.
[12] S. Isam and I. Darwazeh, "On the digital design of non-orthogonal spectrally efficient frequency division multiplexed (FDM) signals*," in 4th Int. Symp. Broadband Commun*. (ISBC'10), Jul. 2010.
[13] S. Isam and I. Darwazeh, "Simple DSP-IDFT techniques for generating spectrally efficient FDM signals," *in IEEE, IET Int. Symp. Commun. Syst., Netw., Digital Signal Process.*, Jul. 2010, pp. 20–24.
[14] S. Ahmed and I. Darwazeh, "IDFT based transmitters for spectrally efficient FDM system," *in Proc. London Commun. Symp.*,Sep.2009