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Zero-Voltage Switching and Zero-Current-Switching Interleaved Boost Converter for reducing Switching Losses

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Abstract

An interleaved boost converter with zero-voltage switching (ZVS) and zero-current switching (ZCS) characteristics is proposed in this project. With this proposed method in addition to decreasing the current stress of the main circuit device, it can able to ripple of the input current and output voltage. In this launching the soft-switching interleaved converter reduces the complexity and cost. To reduce the switching losses main switches can attain the characteristics of ZVS and ZCS consequently. Based on the condition of the duty cycle this converter topology has two operational conditions, to determine these two conditions a driving circuit is proposed. The principle of operation and designed methods of converter is studied and also theoretical analyzed. Simulations results are used to verify the viability and accuracy of the proposed converter.

I. Introduction

An interleaved boost converter is the combination of two or more number of conventional topologies, and with the same power ratings current through the interleaved boost converter is reduced to half of the conventional topology. The main feature of this interleaved boost converter the input current ripple and output voltage ripple are lower than those of the conventional topologies.

The single boost converter can use the zero-voltage switching (ZVS) and/or zero-current switching (ZCS) to minimize the switching loss of the high-frequency switching [1]–[4], [13]–[16], [18]. But, they are considered for the single topology. The interleaved boost converters with ZCS or ZVS are proposed in [5]–[8], [17]. These topologies have higher efficiency than the conventional methods because the proposed circuits reduce the switching losses of the main switches with ZCS or ZVS. However, these circuits to reach soft switching with singly or with more auxiliary circuits can just achieve the junction of ZVS or ZCS. In [9], the soft-switching circuit for the interleaved boost converter is proposed. Nevertheless, its main switches are zero-current turn-ON and zero-voltage turn-OFF and the converter operates in the discontinuous mode. The maximum duty cycle of the converter is also restricted.

In [10], it reduces the voltage stresses of the switches by the double voltage technique with the help of the double-voltage capacitor, but it does not decreases the switching losses of the main switches of the interleaved boost converter by the soft-switching techniques. A soft-switching bridgeless power factor correction circuit is shown in [11]. It is not the abovementioned interleaved boost converter, but it is two conventional boost converters operated in the ac input source. In this common resonant circuit is used there by the resonant elements reduced. There by weight is reduced and also the cost is less. And this topology reduces the switching losses and increases the efficiency by ZVS method, but it does not reduce the turn-OFF switching losses by a ZCS method.

This project proposes an interleaved boost converter with both the zero-voltage turn-ON and zero-current turn-OFF for the main switches to increase the efficiency with a wide range of load. An interleaved boost converter with zero-voltage switching (ZVS) and zero-current switching (ZCS) is the parallel combination of two boost converters and their driving signals stumble 180◦ and this creates the operation assumed symmetrical. In this launching the soft-switching interleaved converter reduces the complexity and cost.

Ii. Analysis of operation

An interleaved boost topology and applies the common soft-switching circuit is shown in fig. 1. To reach the ZVS and ZCS functions resonant circuit consists of the resonant inductor *Lr*, resonant capacitor *Cr*, parasitic capacitors *CSa* and *CSb*, and auxiliary switch *Sr* to develop into a resonant way. The operating

modes of this circuit, depending on the duty cycle of the main switch is shown in fig.2.

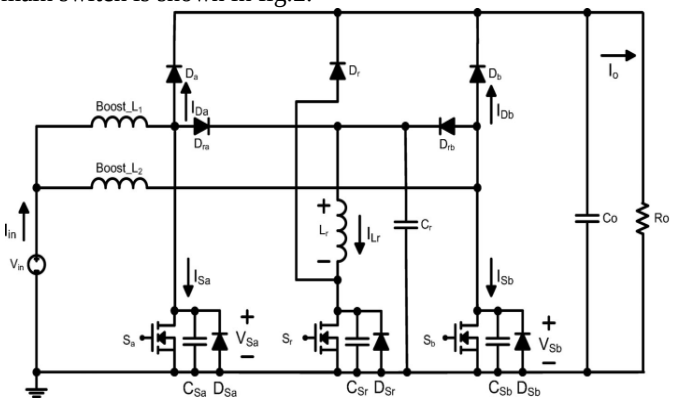


Fig. 1 A novel interleaved boost converter with characteristics of zero-voltage switching and zero-current switching.

A. Operational Analysis of D <50% Mode

In this section the operating principle of the proposed topology is described. There are 24 operational modes in the complete cycle in this mode. Among these 24 operational modes only the 12 modes related to the main switch *Sa* are analyzed, because the interleaved topology is symmetrical. The related waveforms when the duty cycle of the main switch is less than 50% are shown in fig.3. There are some assumptions to simplify the circuit analysis.

1) All power switches and diodes are ideal.
2) The input inductor and output capacitor are ideal.
3) The two inductors are equal; Boost_L1 = Boost_L2 .
4) The duty cycles of the main switches are equal; *D*1 = *D*2 .

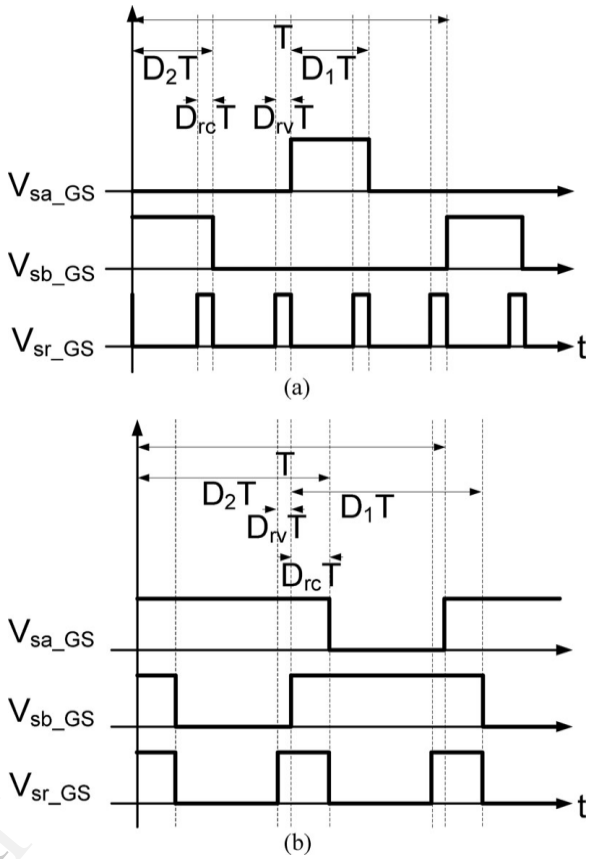
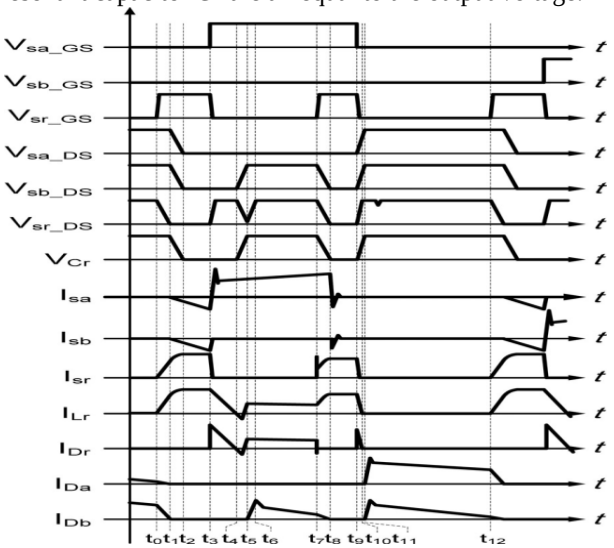


Fig. 2 switching waveforms of the main switches *Sa* and *Sb* and auxiliary switch *Sr*
(a)*D* < 50% mode. (b)*D* > 50% mode.

Mode 1 [t0 –t1]: In this mode, the main switches *Sa* and *Sb* are turned OFF, the auxiliary switch *Sr* and the rectifier diodes *Da* and *Db* are turned ON, and the clamped diode *Dr* is turned OFF, this circuit is shown in fig. 4(a).The voltages across the parasitic capacitors *CSa* and *CSb* of the main switches and the resonant capacitor *Cr* are all equal to the output voltage.



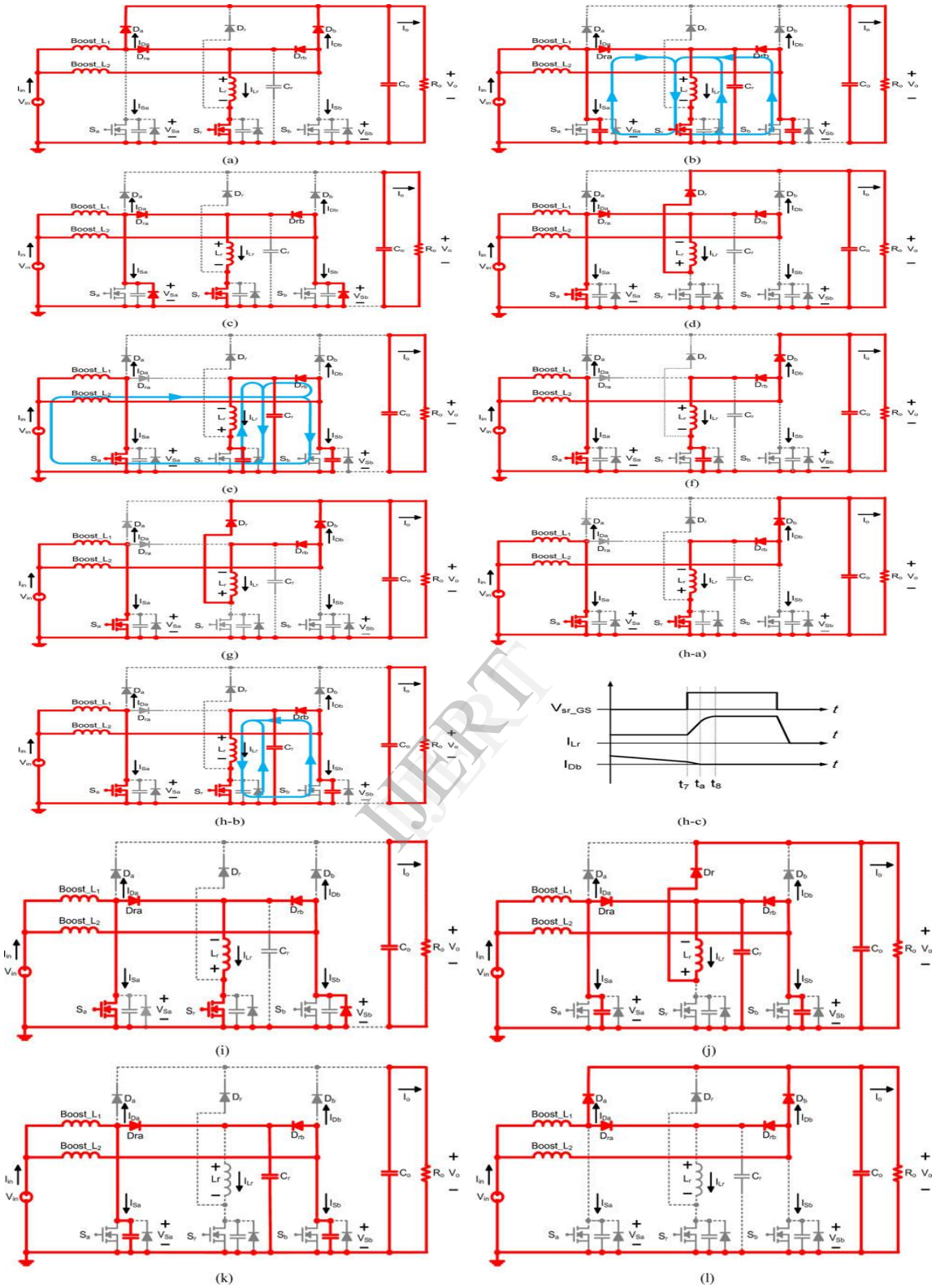


Fig. 4 equivalent circuits of different modes (D < 50%). (a) Mode 1 [$t0$ –$t1$]. (b) Mode 2 [$t1$ –$t2$]. (c) Mode [$t2$ –$t3$]. (d) Mode 4 [$t3$ –$t4$]. (e) Mode 5 [$t4$ –$t5$]. (f) Mode 6 [$t5$ –$t6$] (g) Mode 7 [$t6$ –$t7$]. (h-a) Mode 8 [$t7$ –ta]. (h-b) Mode 8 [ta –$t8$]. (h-c) Detailed waveform of the Mode 8.
(i) Mode 9 [$t8$ –$t9$]. (j) Mode 10 [$t9$ –$t10$]. (k) Mode 11 [$t10$ –$t11$]. (l) Mode 12 [$t11$ –$t1$].

1) Voltage Ratio of D < 50% Mode: The Mode of operation and its equation can be seen [1].Fig. 5(a) shows the real and Fig. 5(b) shows the simplified waveforms of the proposed topology. We can ignore some trivial stages. The

operation for the boost inductor Boost_L1 equivalent circuits is shown in fig. 6. The inductor Boost_L2 has the similar results.

So, when the switch is turned ON, the boost inductor current can be resulting to be

$$\sum_{Sa=on} \Delta i_{L1} = \frac{V_{in} \times \left(\Delta t_{bc} + \Delta t_{dc} + \Delta t_{ef} + \Delta t_{fg} + \Delta t_{hi}\right)}{L_1}$$
$$= \frac{V_{in} \times (D_1 + D_{rc} + 2D_{rv})T}{L_1}. \quad (1)$$

And when the switch is turned OFF, the boost inductor current is

$$\sum_{Sa=off} \Delta i_{L1} = \frac{(V_{in} - V_o) \times \left(\Delta t_{ab} + \Delta t_{cd} + \Delta t_{gh}\right)}{L_1}$$

$$= \frac{(V_{in} - V_o) \times [1 - (D_1 + D_{rc} + 2D_{rv})]T}{L_1}. \quad (2)$$

Then, the voltage conversion ratio can be derived to be

$$\frac{V_o}{V_{in}} = \frac{1}{1 - (D_1 + D_{rc} + 2D_{rv})}. \quad (3)$$

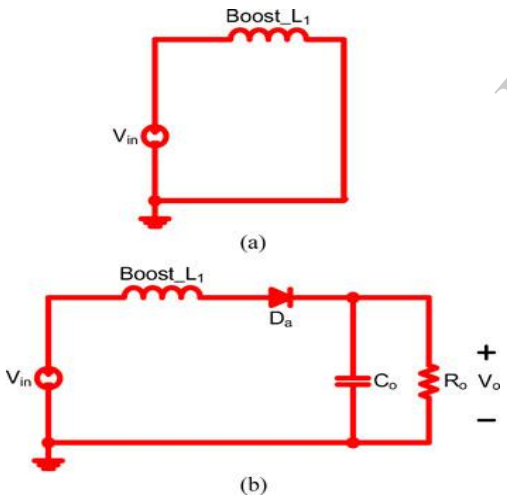


Fig.5 Boost Inductor (*D* < 50).

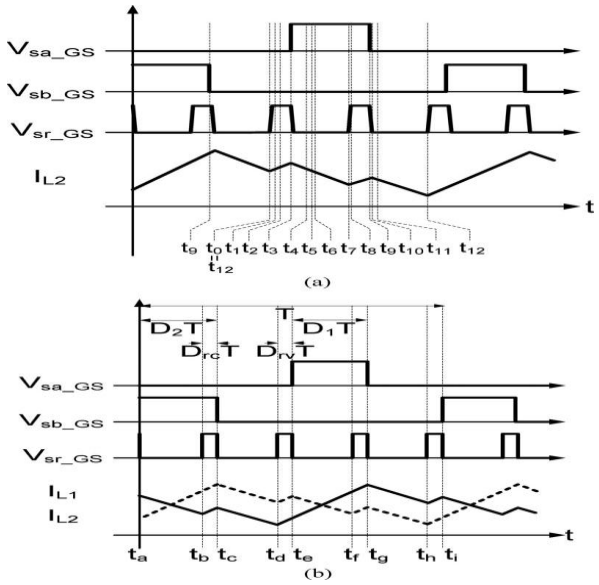


Fig.6 Switching stages (*D* <50%). (a) Real switching stages. (b) Simplified switching stages

2. Operational Analysis of D >50% Mode

In this section describes the principle of the proposed topology operated in *D* > 50%.

There are 14 operational modes in the complete cycle in this mode. Among these 14 operational modes only the 12 modes related to the main switch *Sa* are analyzed, because the interleaved topology is symmetrical. When the duty cycle of the main switch is more than 50% the corresponding waveform is shown in fig. 7.

*Mode 1 [t*0 *–t*1 *]:* Fig. 8(a) shows the equivalent circuit of this mode. In this mode of operation all switches *Sa* , *Sb* , and *Sr* are turned ON, and the rectifier diodes *Da* and *Db* and clamped diode *Dr* are turned OFF. The main switch currents *ISa* and *ISb* are less than or equal to zero while the previous mode ends. if the condition in (24) can met then the main switch *Sb* can attain the ZCS characteristic at *t* = *t*1.

The gap time *t*01 and the resonant inductor current are

$$t_{01} = (D_1 - t_{07})T = (D_1 - 0.5)T \quad (4)$$

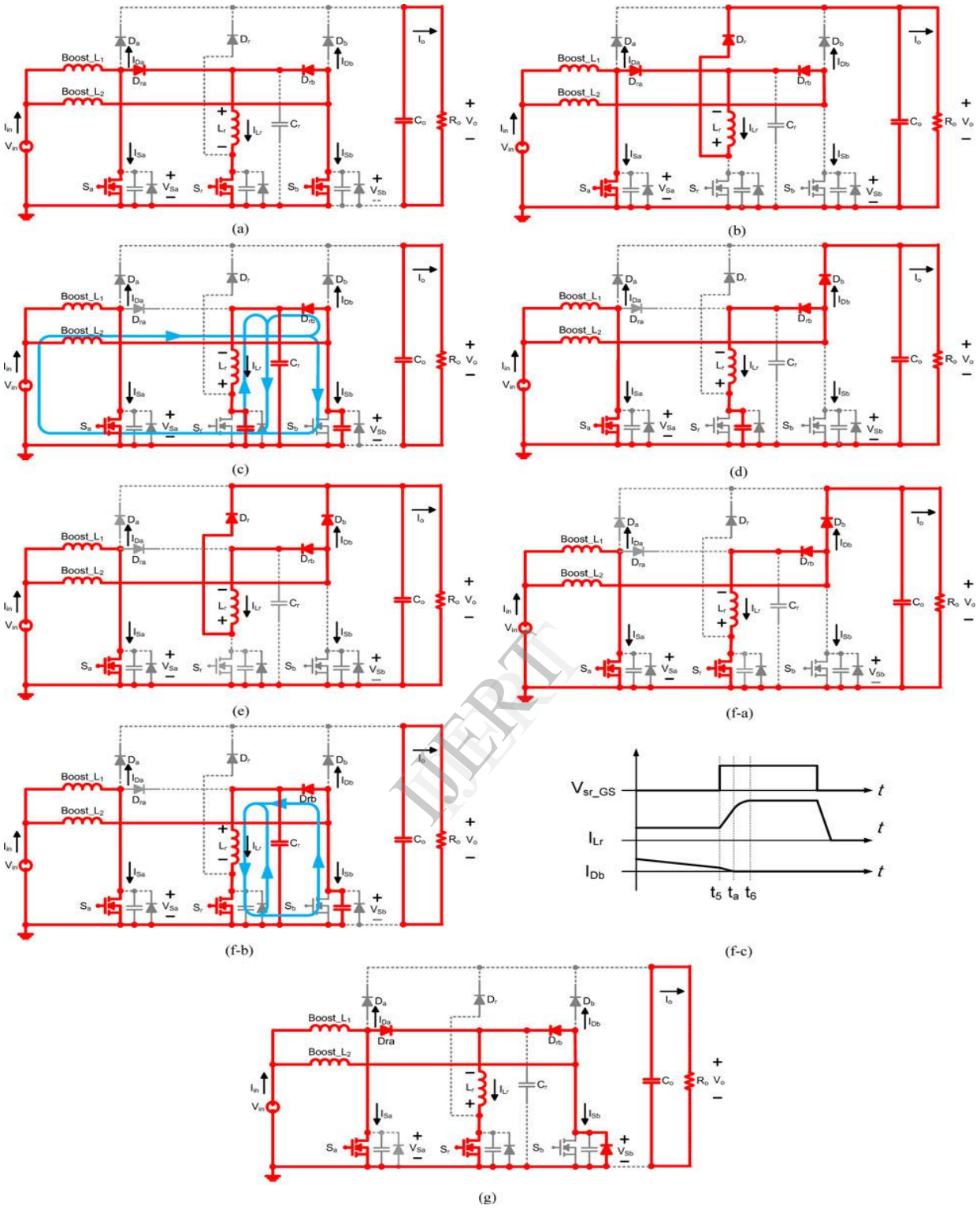


Fig. 8 Equivalent circuits of different modes (D > 50%). (a) Mode 1 [$t0$ –$t1$]. (b) Mode 2 [$t1$ –$t2$]. (c) Mode 3 [$t2$ – $t3$]. (d) Mode 4 [$t3$ –$t4$]. (e) Mode 5 [$t4$ –$t5$]. (f-a) Mode 6 [$t5$ –ta]. (f-b) Mode 6 [ta –$t6$]. (f-c) Detailed waveform of the Mode 6. (g) Mode 7 [$t6$ –$t7$].

Mode 2 [t1 –t2]: The energy stored in the resonant inductor *Lr* is relocated to the output load by the clamped diode *Dr* , because the auxiliary switch *Sr* is turned OFF. When the resonant inductor current *ILr* reduces linearly until it reaches zero at $t = t2$, the clamped diode *Dr* is turned OFF.

The interval time *t*12 is

$$t_{12} = L_r.\frac{I_{in}}{V_o}. \quad (5)$$

*Mode 3 [t*2 *–t*3 *]:* The clamped diode *Dr* is turned OFF in this mode. The energy stored in the boost_L2 and the energy stored in the parasitic capacitor *CSr* of the auxiliary switch are moved to the resonant inductor *Lr*, resonant capacitor *Cr*, and parasitic capacitor *CSb* of the main switch at this situation. The rectifier diode *Db* is turned ON when the main switch voltage *VSb* and resonant capacitor voltage *VCr* improved to *Vo* at *t* = *t*3.

The resonant inductor current is

$$i_{Lr}(t) = -V_o\sqrt{\frac{CC_{Sr}}{L_r(C+C_{Sr})}}\,sin\sqrt{\frac{C+C_{Sr}}{L_rCC_{Sr}}}t + \frac{I_{L2}C_{Sr}}{C+C_{Sr}} \times\left(1-cos\sqrt{\frac{C+C_{Sr}}{L_rCC_{Sr}}}t\right). \quad (6)$$

The resonant time *t*23 is

$$t_{23} = \pi\sqrt{\frac{L_rCC_{Sr}}{C+C_{Sr}}}. \quad (7)$$

*Mode 4 [t*3 *–t*4 *]:*The parasitic capacitor *CSr* of the auxiliary switch is linearly charged by *IL* 2 − *Io* to *Vo* at t>t3. Then, the clamped diode *Dr* is turned ON at *t*4.

The interval time *t*34 is

$$t_{34} = \frac{C_{Sr}.V_o}{I_{L2}-I_o}. \quad (8)$$

*Mode 5 [t*4 *–t*5 *]:* Fig. 8(e) shows the equivalent circuit of this mode. The clamped diode *Dr* is turned ON at t4. The energy stored in the inductor *Lr* is transmitted to the output load by the clamped diode *Dr*. The clamped diode *Dr* is turned OFF when the auxiliary switch *Sr* is turned ON at *t* reaches to *t*5.

The interval time *t*45 and the resonant inductor current are

$$t_{45} = 0.5T - t_{04} - D_{rv}T \quad (9)$$

$$i_{Lr}(t_5) \approx i_{Lr}(t_4). \quad (10)$$

*Mode 6 [t*5 *–t*6 *]:* the equivalent circuit and the detailed waveform are shown in Fig. 8(f-a) and Fig. 8(f-c) respectively. In the interval [*t*5*– ta*], the resonant inductor current *ILr* raises linearly until it reaches *IL* 2 and the rectifier diode current *IDb* reduced to zero at *t* = *ta* , then the rectifier diode *Db* is turned OFF.

The interval time *t*5*a* is

$$t_{5a} = L_r.\frac{I_o}{V_o}. \quad (11)$$

Fig. 8(f-b) shows the equivalent circuit for the interval time [*ta–t*6]. The resonant inductor current linearly increases to the peak value and the main switch voltage *VSb* reduced to zero because of the resonance among *CSb*, *Cr* , and *Lr*. At *t*6, the body diode *DSb* of *Sb* is turned ON.

The interval time *t*6*a* is

$$t_{a6} = \frac{\pi}{2\omega_1} = \frac{\pi}{2}.\sqrt{L_r(C_{Sb}+C_r)}. \quad (12)$$

And the interval time *t*56 is

$$t_{56} = t_{5a} + t_{a6} = L_r.\frac{I_o}{V_o} + \frac{\pi}{2}.\sqrt{L_r(C_{Sb}+C_r)}. \quad (13)$$

*Mode 7 [t*6 *–t*7 *]:* While the resonant capacitor voltage *VCr* and the main switch voltage *VSb* are equal to zero, the body diode *DSb* of *Sb* is turned ON. After this Mode 7 will start. In this mode of operation the resonant inductor current *ILr* is equal to a constant current source. If the condition of *iLr* (*t*6) ≈ *iLr* (*t*7) ≥ *I*in satisfies, the main switch currents *ISa* and *ISb* can be less than or equal to zero. Then, the main switch *Sa* can be turned OFF beneath the ZCS condition. Due to the conduction of the body diode *DSb* in this mode the main switch *Sb* reaches ZVS. The interval time *t*67 is

$$t_{67} = 0.5T - t_{06}. \quad (14)$$

And the zero-current switching conditions are

$$i_{Lr}(t) = i_{Lr}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{sb}+C_r)}} \geq I_{in}(t) \quad (15)$$

2) The duty time of ZCS is longer than the interval time *t*56 (*DrcT* > *t*56).

1) Voltage ratio of D > 50% Mode: The real waveforms and the simplified waveforms in this mode are shown in fig.9(a)and fig,9(b) respectively . The operation for the boost inductor Boost_L1 equivalent circuit is shown in fig. 10.

When the switch is turned ON, the boost inductor current is

$$\sum_{Sa=on} \Delta i_{L1} = \frac{V_{in} \times (\Delta t_{ab} + \Delta t_{bc} + \Delta t_{cd} + \Delta t_{de} + \Delta t_{fg})}{L_1} = \frac{V_{in} \times (D_1 + D_{rv})T}{L_1}. \quad (16)$$

And when the switch is turned OFF, the boost inductor current is

$$\sum_{Sa=off} \Delta i_{L1} = \frac{(V_{in} - V_o) \times (\Delta t_{ab} + \Delta t_{cd} + \Delta t_{gh})}{L_1} = \frac{(V_{in} - V_o) \times [1 - (D_1 + D_{rc} + 2D_{rv})]T}{L_1}. \quad (17)$$

Then, the voltage conversion ratio can be derived to be

$$\frac{V_o}{V_{in}} = \frac{1}{1-(D_1+D_{rv})}. \quad (18)$$

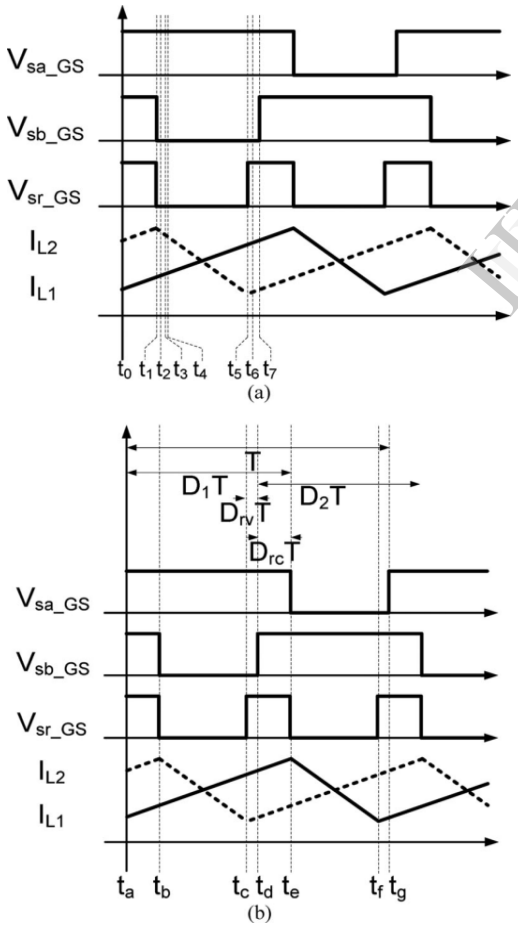


Fig. 9 switching waveforms (*D* > 50%). (a) Real waveforms. (b) Simplified waveforms.

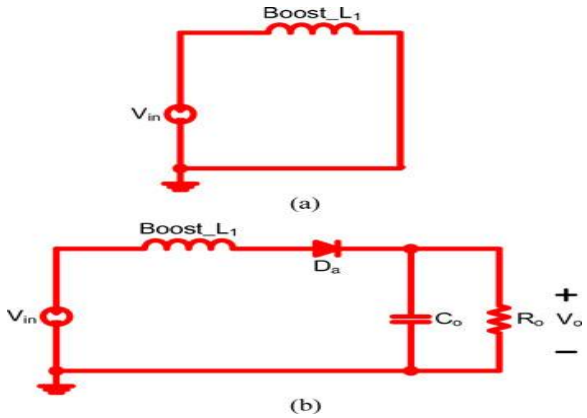


Fig. 10 Equivalent circuits for the boost inductor (*D* >50%).

III. Simulation Results

(i) D > 50%

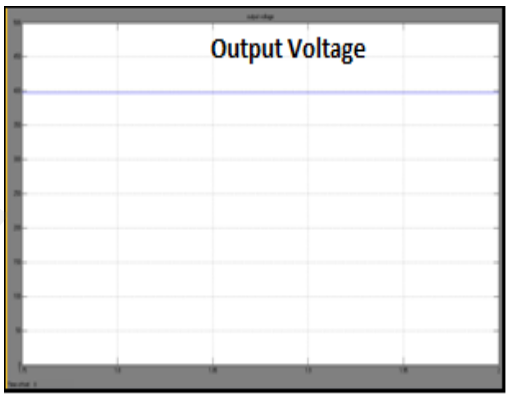


Fig.11(a) Output Voltage

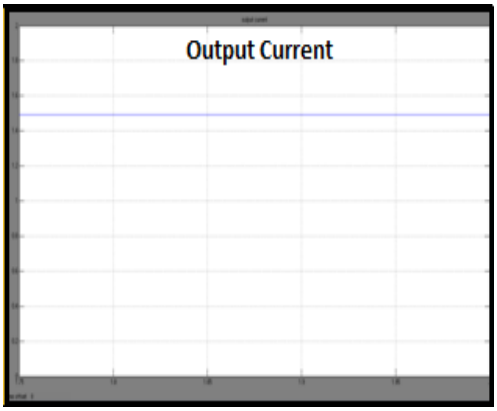


Fig.11(b)Output Current

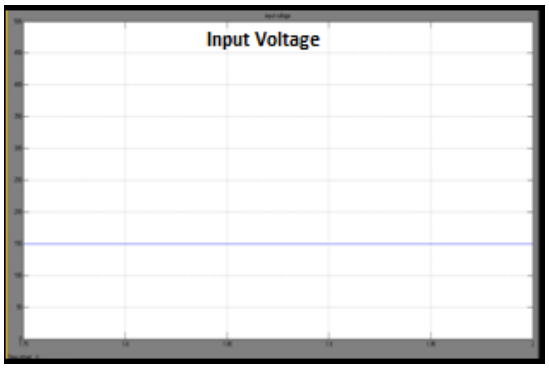


Fig.11(c)Input Voltage

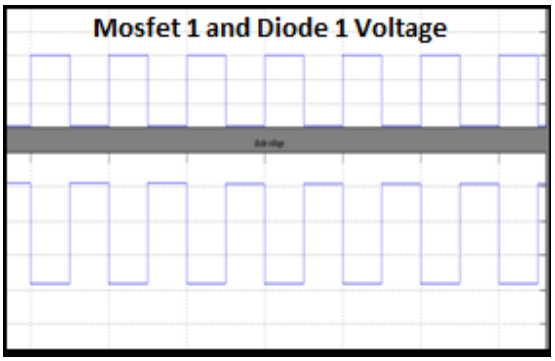


Fig.11(d) Mosfet 1 and Diode 1 Voltage

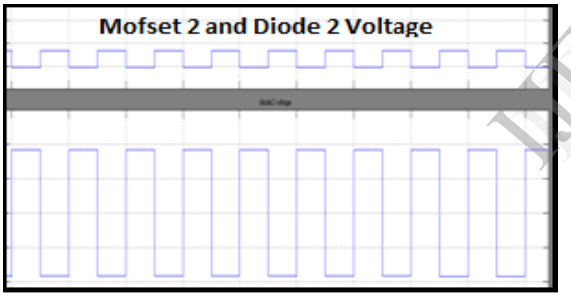


Fig.11(e)Mosfet 2 and Diode 2 Voltage

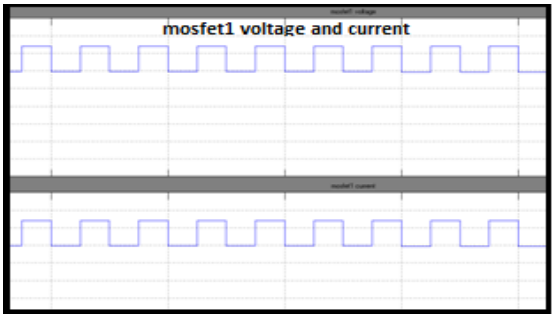


Fig.11(f)Mosfet1 voltage and current

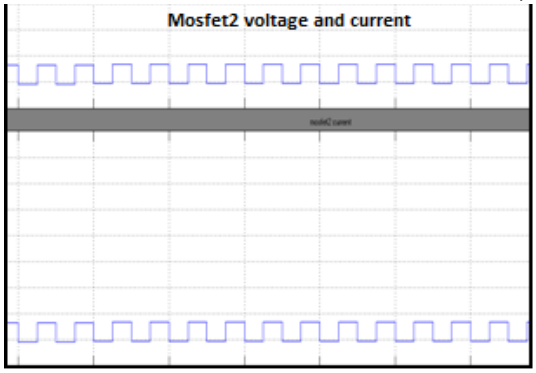


Fig.11(g)Mosfet2 voltage and current

II (D<50%) Mode

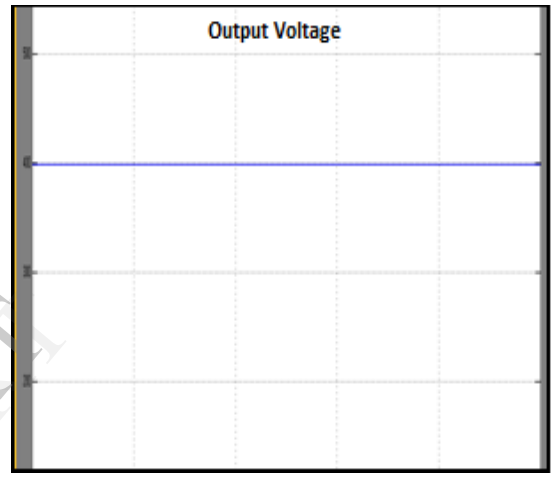


Fig.11(h)Output Voltage

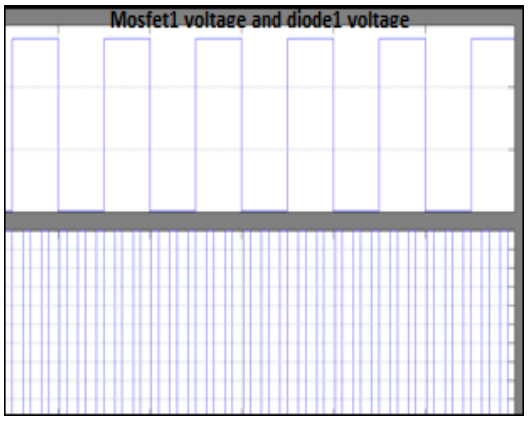


Fig.11(i)Mosfet1 voltage and diode1 voltage

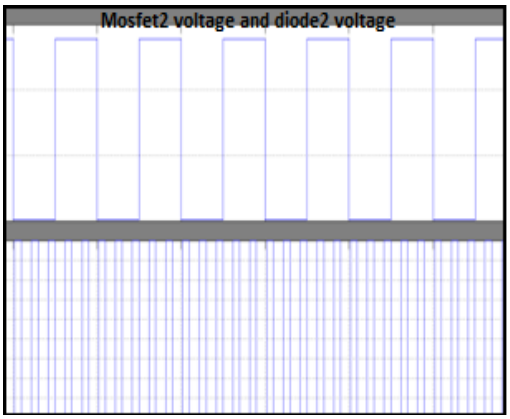


Fig.11(j)Mosfet2 voltage and diode2 voltage

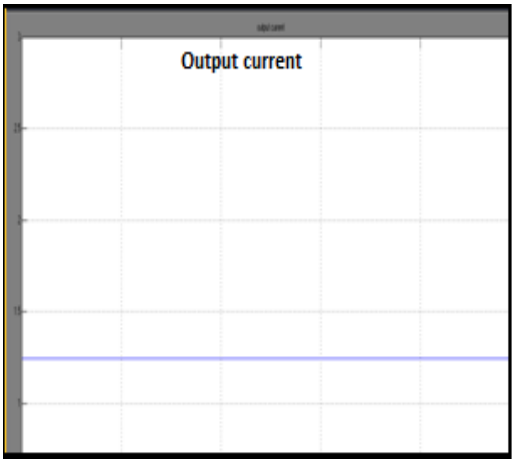


Fig.11(k)Output current

Iv. Conclusion

A novel interleaved boost converter with zero-voltage switching and zero-current-switching functions is proposed in this project. The duty cycle of this proposed topology can be more or less than 50%. It has many characteristics. The main switches *Sa* and *Sb* can achieve both ZVS and ZCS conditions. With this method achieve the voltage stress of all switches is equal to the output voltage. The switching functions ZVS or ZCS function can be achieved just by the adjustment of the driving circuit. The efficiency of this topology is improved to 95.5% with output power of 400W and input voltage of 250V.

V. References

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