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Zero Voltage Switching in a Low Voltage High Current DC-DC Converter

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***Abstract*—In the present trend of power electronics, output voltages in the range of 1.8V to 5V is preferred in order to reduce the size of the circuit and to increase the efficiency. For example a LED TV uses voltage stepped down to around 1.5 or 2 V which helps in making the internal components small and compact which results in reducing the size of the TV unlike older models. The circuit is designed for high current-low voltage output where the voltage is designed to be 2.5V output.**

This paper gives the design, implementation and test results of a high efficiency, high power density isolated DC-DC converter operating at constant frequency (200 KHz) for Low Voltage High Current (LVHC) applications. The initial design of this dc-dc converter is implemented with PWM based Forward Topology using schottky diodes for forward conduction and freewheeling action. The isolation between the output and input is achieved by isolating the transformer primary and secondary with the use of power ground and digital ground in the feedback loop to regulate the output voltage. The efficiency of DC-DC converter is improved by implementing the "ZVS" for eliminating the switching loss. The comparison in converter efficiency without ZVS and when ZVS is implemented is observed.

Index Terms- LVHC DC-DC CONVERTER, ZERO VOLATGE SWITCHING, EFFICIENCY.

I. INTRODUCTION

A dc-dc buck converter reduces the voltage to the regulated 5 V or 3.3 V required by the processor ICs. High efficiency is a necessity and the process of cooling of inefficient power converters is difficult and expensive. The ideal dc-dc converter exhibits 100% efficiency; practically, efficiencies of 70% to 95% are typically obtained. This is achieved using switched-mode power supplies, or chopper circuits whose elements dissipate negligible amount of power. Pulse-width modulation (PWM) allows control and regulation of the converter total output voltage. The proposed paper consists of a converter with input specifications of 26-42V and output specifications of 2.5V/5A. It is operated at high frequencies of 200KHz in order to reduce losses.

The topology selection for low output voltage, high current application is mainly based on high-power-density and minimum size of the converter. Generally power conversion with a large step-down ratio such as from 42 V to below 5V, can be efficiently performed only in topologies with a step-down transformer as done in a Forward converter. Forward converter with resonant reset is selected for this application because of the following reasons:

- Simplest topology – results in smaller or lesser components as compared to Flyback, Push Pull, Half-Bridge, Full-Bridge converters.
- Forward converter provides less noise at the outputs and has no right-half plane zero in the control loop.
- Compared to the Push-Pull topology, the Forward Converter has only one power switch and does not have any flux imbalance problems as the push-pull converter
- There are no resonant components since the resonant stage to reset the transformer is carried out by the transformer magnetizing inductance and the semiconductor parasitic capacitances.
- There is no demagnetizing winding or demagnetizing network.
- Schottky rectifiers are used at the output stage to keep the circuit simple.
- Based on the prior experience with 20W DC/DC converter, Forward topology is selected with voltage mode control (1524B controller IC).

In order to further improve the efficiency of the converter employs active clamping technique and the switching losses also have to be improved. This paper explains the Zero Voltage Switching method employed in the converter in order to reduce the switching loss and enhance the efficiency.

II. PROPOSED SYSTEM

The figure 1 shown below is the proposed block diagram of the converter .The converter gets its input from a raw bus system , which goes through various blocks like start up circuit, rectifier filter, PWM IC , current transformer and then to the output load.

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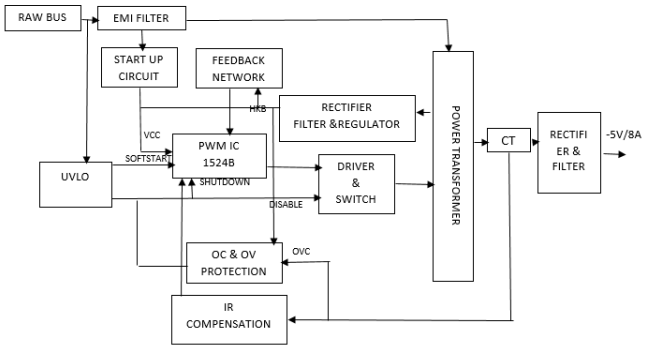

Fig 1. Proposed system block diagram

III. MODEL DESCRIPTION OF ARCHITECTURE :

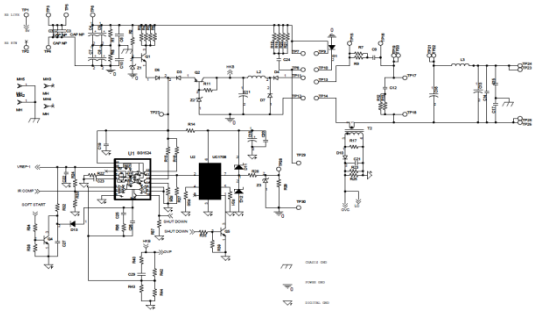

Fig 2. Schematic model of the LVHC DC-DC converter.

The converter set-up is as shown in the figure 2, the circuit of the block described in section II are shown here.

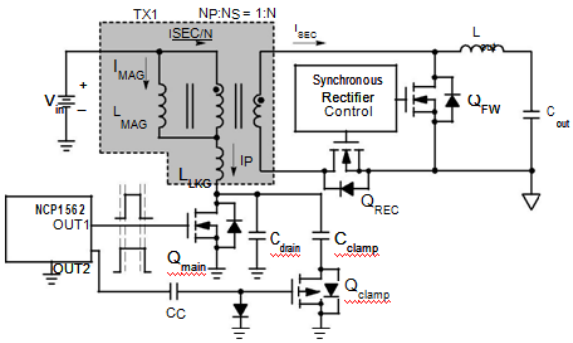

Fig 3.Circuit diagram of the ZVS circuit with active clamp feature.

Figure 3 shows the active clamp ZVS circuit which implements the zero voltage switching technique in the converter to ensure that the switch operates at zero voltage so that the power dissipation is close to zero and efficiency is considerably improved. The clamp MosFET is a P-channel MosFET whose drain is connected to the drain of N-channel MosFET , this circuit reduces the ON time

IV. DESIGN OF THE CONVERTER

i. CONVERTER

As we know that it is very important to operate the converter at high switching frequency in order to reduce the losses and also to enhance the efficiency. The switching losses are eliminated by Zero Voltage Switching (ZVS).

ii. ZVS CIRCUIT

Fig 3 shows the circuit diagram of the ZVS circuit which makes the MosFET switch to turn ON at zero voltage thereby reducing losses and enhancing efficiency .

V. BUCK CONVERTER :

A buck converter is a dc to dc power converter with output voltage is less than input voltage this can be achieved by duty cycle of the switch (d<0.5) switch may be IGBT, MosFET, BJT etc... The buck converter contains at least two semiconductor devices. The output of the buck converter is given to the load. The active clamp PWM IC gives the PWM pulses to the MosFET to maintain constant output voltage.

VI. DESIGN

The following are the design formulae of the converter which explains about the transformer design , capacitor and inductor design used in the converter: **POWER TRANSFORMER DESIGN**

To find the area product of the core required($W_a A_c$), the formula used is:

$$P=0.005B_{max}F_sW_aA_c/D_{cma}$$

(i) Primary winding

To operate the core at 700G (from catalog, Bmax allowed for ferrite core @200 KHz = 700 G), the turns required in primary winding:

$$V=NA_e(dB/dt)*10^{(-8)}$$

Assuming efficiency of 65%

Pin = 13/0.65 =20W

Iin,pk = Iin(dc),max/Dmax

$$I_{prms}=I_{in,pk}\sqrt{D_{max}}$$

(ii) +5V O/P Secondary winding

Rectifier diode selected is 16CYQ100. Considering V_f = 0.7V

$$V_o=\left[\frac{N_{s1}(25-0.55)}{N_p}-0.7\right]D \qquad \text{--- (3.3.1.4)}$$

Secondary rms current, $I_{s,rms}=I_{s1}\sqrt{D_{max}}$

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(iii)Reset winding

The number of turns will be same as the primary winding. = **25**

Since the magnetizing current is very small, so single 35AWG wire can be used

The winding details of the transformer can be summarized as follows:

OUTPUT INDUCTOR DESIGN

I.+5V O/P LINE FIRST FILTER INDUCTOR

Calculating the value of filter inductor from the above values,

$$(V_o+V_f)=L(\Delta I/T_{off})$$

ΔI = 20% of Full Load Current

Current through inductor = DC current + RMS current

II. +5V O/P SECOND FILTER INDUCTOR

$1/(2\pi\sqrt{L02C})$

III. HKB INDUCTOR

$$(V_o+V_f)=L(\Delta I/T_{off})$$

ΔI = 0.07A

New no. of turns, **N** = $\frac{120}{\sqrt{0.98}}$ **= 121.21 ≈121 (write equation)**

O/P FILTER CAPACITOR DESIGN

1. **+5V O/P FIRST STAGE FILTER CAPACITOR (WRITE ONE LINE HOW U SELECT)**

Rms current through I stage filter capacitor = 0.288A

Derated voltage rating of the capacitor required = 2 x 5 = 10V. The derating factor of 3 suggested for solid tantalum capacitors has been taken.

Capacitor selected: **68uF, 15V (CWR29, Case H**. Since H style has lower ESR than G style)

No. Of capacitors required in parallel= 0.288/0.82 = 0.4= 1

2. **+5V O/P SECOND STAGE FILTER CAPACITOR(WRITE ONE LINE HOW U SELECT)**

Rms current through II stage filter capacitor = 0.012A

Derated voltage rating of the capacitor required = 2 x 5 = 10V. The derating factor of 3 suggested for solid tantalum capacitors has been taken.

Capacitor selected: **68uF, 15V (CWR29, Case H)** is selected.

No. Of capacitors: 1

3. **HKB FILTER CAPACITOR(WRITE ONE LINE HOW U SELECT)**

Rms current through capacitor = 0.011A

Derated voltage rating of the capacitor required = 2 x 13 = 26

Capacitor selected: **1uF, 35V (CWR29, CaseD)** is selected. The derating factor of approx. 3, suggested for solid tantalum capacitors has been taken.

No. Of capacitors required in parallel = 0.011/0.17 = 0.064 = 1

With the above design calculations the converter is designed and is tested at different values of input voltage and load current

ZERO VOLTAGE SWITCHING

The following is the design formulae for the zero voltage switching circuit:

The zvs technique makes the switch to turn on only when the voltage has dropped to zero thereby reducing switching losses and increasing efficiency.

The magnetizing current charges and discharges the clamp capacitor every cycle and is given by the equation,

$$I_{MAG}=(V_{in}*D)/(f_{SW}*L_{MAG})$$

Using the above values Imag= 88.4172mA.

It is absolutely critical to consider the ripple current rating in the selection of Cclamp. Otherwise the capacitor may overheat. The minimum ripple current rating of Cclamp is determined by the magnetizing rms current. Assuming the magnetizing current reverses halfway during the OFF-time, the clamp capacitor rms current is approximated by,

$$I_{Cclamp(rms)}=(V_{in}*D/f_{sw}*L_{MAG})*(\sqrt{[(1-D)/2]})$$

Using the above values,

ICclamp=52.3083mA

Calculating the voltage ripple at drain-source,

Vds ripple= 10% *2*42 =8.4V

CLAMP CAPACITOR

Clamp capacitance from graph @8.4V Vds ripple and high line (42) = 14.5nF to 15nF.

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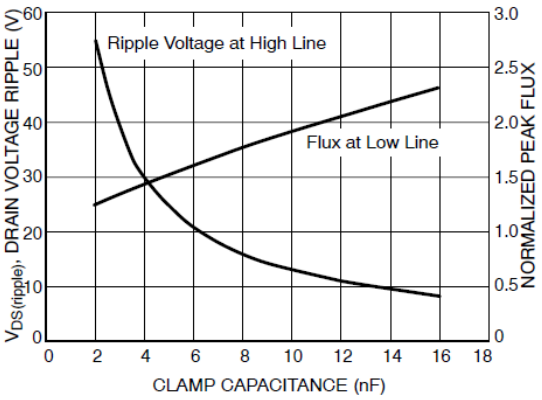


From calculation,

Cclamp [dv/dt] = ICclamp

Using the above values, **Cclamp=12.3671nF.**

COUPLING CAPACITOR

$$C_C= (Q_G/\Delta V_C)+[(V_{DRV}*(1-D)*D)/(\Delta V_C*R_{GS}*f_{sw})]$$

From the above values ,

Cc=51.4KPf

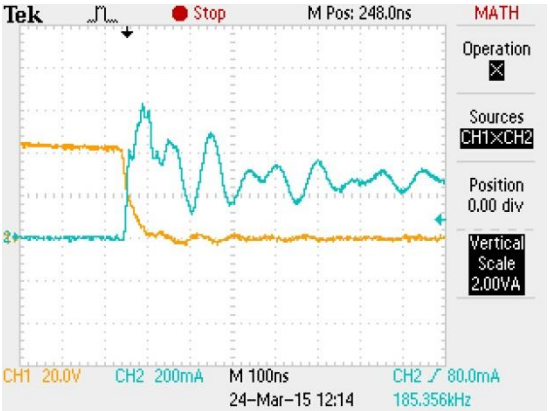
Selection of MOSFET,

The Qclamp Mosfet made use of in the circuit of ZVS is IRF9610 which is a P-channel switch with high Rds ON value of 3Ω , this configuration is a low side active clamp topology.

With the above calculations a LVHC(low voltage high current dc-dc converter) is designed and ZVS is implemented to enhance the efficiency.

VII. EXPERIMENT RESULTS AND WAVEFORMS

The waveform shown below is for two conditions of switching, comparing the switching condition during ZVS and without ZVS.



The above waveform is the converter switching condition when ZVS circuit is not connected. It clearly shows that the current rises before the voltage can drop thereby giving rise to switching losses which reduces the converter efficiency.

The efficiency here ranges between 38% to 55%.

The above designed ZVS circuit was connected to the converter circuit and waveform was observed, it is seen that at zero voltage the current rises , which reduces the losses considerably.

The efficiency here ranges between 60% to 70 %

VIII. CONCLUSION

The LVHC buck converter is being presented wherein the output voltage is as low as 2.5V, suitable for the present day power electronic devices and power applications. The converter was designed and tested without ZVS circuit and then the ZVS circuit was designed, connected to the converter and tested and an improvement in efficiency was observed. The circuit is designed for a constant frequency and the concept of power ground and digital ground is employed in the feedback path for providing the isolation between the primary and secondary. However, the circuit has low efficiency due to switching losses and diode rectifier losses.

As a part of the objective of this paper these losses have to be rectified in order to increase the efficiency. The PWM IC present in the initial design of converter was replaced with an active clamping PWM IC by implementing certain design modifications in the switch, oscillator, duty ratio etc, in order to achieve ZVS (zero voltage switching) so as to minimize losses and achieve higher efficiency. The ZVS technique that is employed in the switching of the MosFET helps in improving the overall efficiency of the circuit upto 70%.

IX FUTURE SCOPE

Further improvement in efficiency can be observed by implementing synchronous rectification where the schottky diodes are replaced by switching devices like MosFET which reduces the diode drop resulting in improving the efficiency of the proposed converter.

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