Zero Voltage Switching In Practical Active Clamp Forward Converter

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ABSTRACT

In this paper; zero voltage switching in active clamp forward converter is investigated. The investigation starts with discussing the basic switching methods: hard switching and soft switching. The concept of ZVS quasi resonant and active clamp reset mechanism is also discussed in detail. A 50W active clamp forward converter with voltage input 16-50V is implemented. The main mosfet switching waveform is analyzed under zero voltage condition.

1 INTRODUCTION

The main issues related to device stresses associated with hard switching are the semiconductor losses due to the finite duration of the switching transients and the electromagnetic compatibility (EMC) problems associated with the high voltage derivative with respect to time, occurring especially at the turn-off transient. Reduction of size and weight of converter systems require higher operating frequencies, which would reduce sizes of inductors and capacitors. However, stresses on devices are heavily influenced by the switching frequencies accompanied by their switching losses. Soft switching techniques use resonant techniques to switch ON at zero voltage and to switch OFF at zero current. There are negligible switching losses in the devices, though there is a significant rise in conduction losses.

In this paper ZVS quasi resonant converter and active clamp concept with switching fundamentals are discussed in detail. Theoretically it is claim that with active clamp mechanism; ZVS could be achieve during turn on and turn off of the main switch. A 50W active clamp forward converter with input voltage range 16-50V is implemented. The aim is to analyze the switching transients at, or close to, zero voltage across the semiconductor devices so as to achieve zero, or low, switching losses. However, it is found that during turn ON the main MOSFET did not switch at zero voltage and this is also discussed.

2 HARD SWITCHING

One of the most basic transistor bridge configurations for power electronic applications is the step down converter. It consists of a voltage source, a power transistor (IGBT in this case) and a freewheeling diode, see Fig. 1. Since this is a voltage source converter, the load is a current source, i.e. inductive. When the switch state is changed from on to off (turn-off) or from off to on (turn-on), the transition will take a finite time in the non-ideal case.

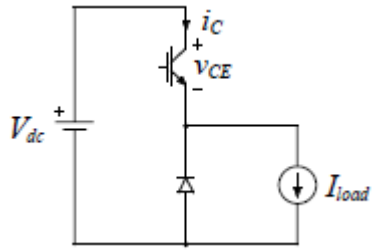


Fig 1. Basic step down converter

Fig. 2 shows typical collector current, ic and collector-emitter voltage, Vce for IGBT, when used in the step down converter above.

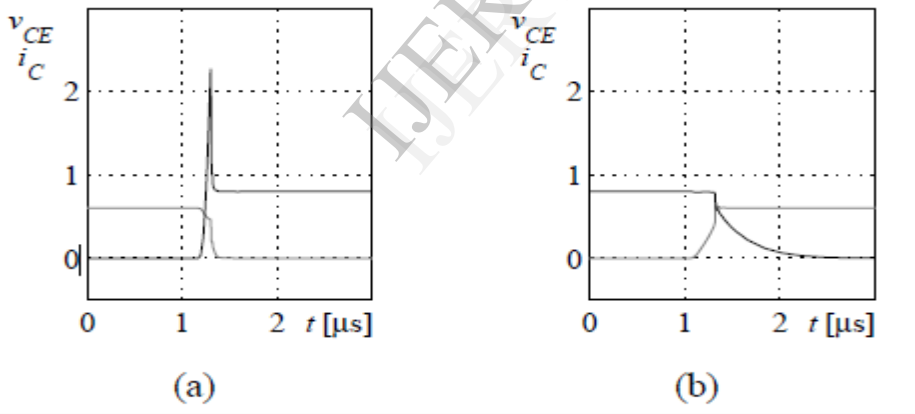


Fig. 2 Transistor current (black) and voltage (grey) at (a) turn-on and (b) turn-off of the power transistor in the step down converter.

In Fig. 2, the IGBT is exposed to a current spike at turn-on due to reverse recovery of the freewheeling diode. It is seen that the IGBT is exposed to simultaneously high current and voltage during the switching transients. This causes high switching losses, especially at turn-off since the IGBT exhibits a collector current tail there.

3 SOFT SWITCHING

To partly overcome the previously mentioned problems in hard switching and to use the semiconductor devices in a more efficient way, soft switching techniques are introduced [5]. Soft switching technique is to shape the voltage or the current waveform by creating a resonant condition so as to force the voltage across the switching device to drop to zero before turning it ON (Zero-Voltage Switching); force the current through the switching device to drop to zero before turning it OFF (Zero-Current Switching); as shown in fig. 3.

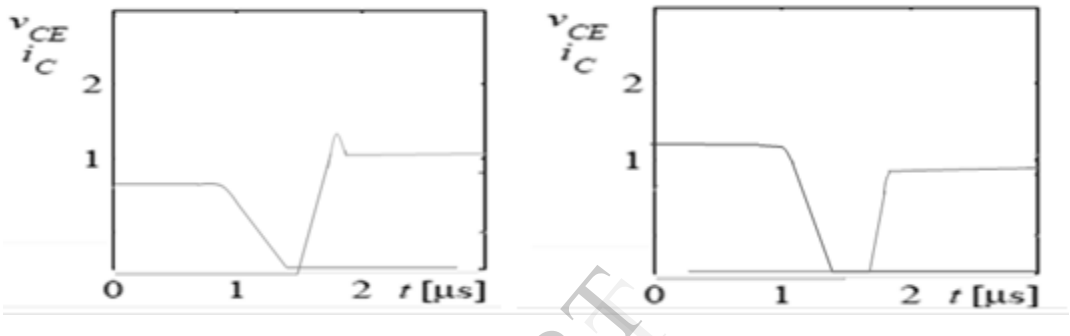


Fig. 3 Transistor current and voltage at (a) turn-on and (b) turn-off of the power transistor in the step down converter (Soft switching).

Hard switching and its consequences have been discussed above. Reduction of size and weight of converter systems require higher operating frequencies, which would reduce sizes of inductors and capacitors. However, stresses on devices are heavily influenced by the switching frequencies accompanied by their switching losses. As the switching losses during switching transient are highly reduced in case of soft switching; the advantage of operating dc-dc converters in higher operating frequencies can be utilized with soft switching techniques.

The detail concept of soft switching; how ZVS is achieved using resonant circuit in converters; is explained taking ZVS quasi resonant buck converter [2] as an example in the following section.

4 ZERO VOLTAGE SWITCHING QUASI RESONANT CONVERTER

Fig. 4a shows the ZVS-QR Buck converter. Here the resonant circuit is formed by the capacitor Cr and inductor Lr. During the steady-state operation and if the bulk energy storage components, LF and CF, are large, the analysis can be simplified by assuming the current through the bulk inductor is a current sink. Because the average current through CF is zero in steady-state, the average currents of LF and Io are equal. Hence the ZVS-QR Buck converter can be redrawn in Fig. 4b for simplification during analysis.

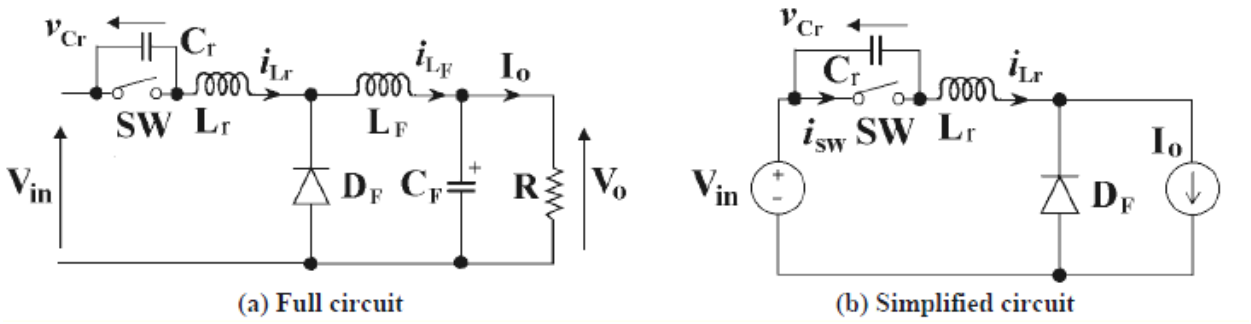


Fig.4 ZVS-QR Buck converter

The circuit can be considered in four equivalent circuits that depend on the switching device SW and diode's on- and off-states. There are four states of operation and the time domain waveform is shown in Fig. 5.

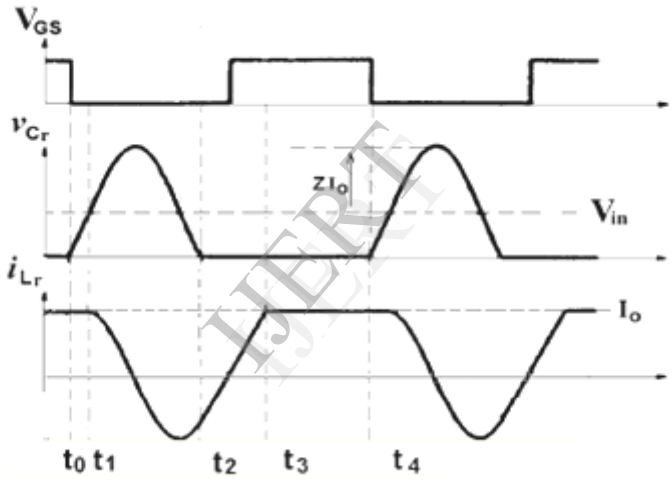
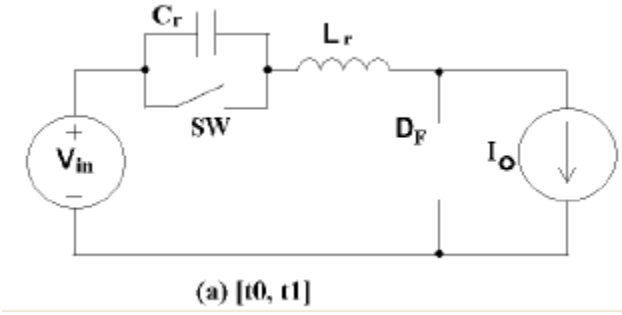


Fig. 5 Idealized waveforms of the ZVS-QR Buck converter

A) Capacitor charging stage [t0, t1]:



Switch SW is turned off at t0. Input current i_{Lr} rises linearly and is governed by the state equations:

$$C_r \frac{dV_C}{dt} = I_o$$

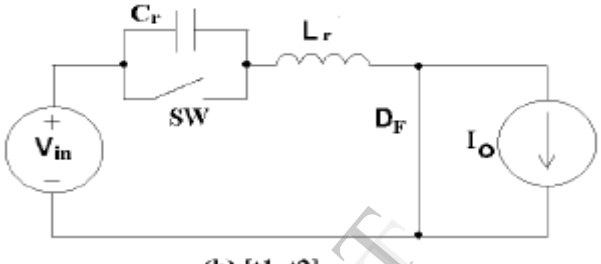
Solution: $$v_{Cr} = \frac{I_o(t - t_0)}{C_r}$$

When v_{Cr} increases to Vin, the voltage across D_F becomes positive and it is in forward bias.

The duration of this state $T_{d1} = C_r V_{in} / I_o$

Boundary condition: $v_{Cr} = V_{in}$

B) Resonant state [t1, t2]:



(b) [t1, t2]

L_r and C_r resonate and D_F is on. The state equations are:

The solution is:

$$v_{Cr} = V_{in} + ZI_o \sin \omega_o (t - t_1)$$
$$i_{Lr} = I_o \cos \omega_o (t - t_1)$$

where

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}$$
$$Z = \sqrt{\frac{L_r}{C_r}}$$

The duration of this state T_{d2} is

$$\frac{\alpha}{\omega_o} \text{ where } \alpha = \sin^{-1} - \Phi = \sin^{-1} \frac{-V_{in}}{ZI_o}$$

The switch SW consists of transistor T and diode D as shown in Fig. 6.

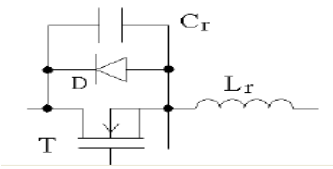
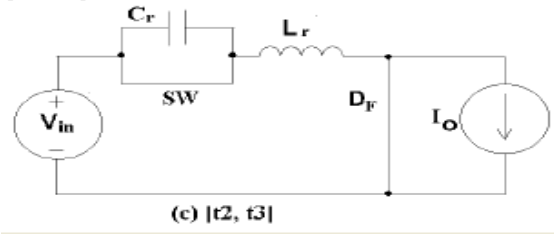


Fig. 6 Configuration of the zero-voltage switch

When resonant voltage v_{Cr} reaches zero, it cannot be reversed because the anti-parallel diode D of the switch conducts. The transistor T of the switch SW can be turned on after that to achieve zero-voltage switching.

C) Inductor recovering stage [t2, t3]:



Resonance stops, Lr begins to be charged by the input voltage Vin.

$$L_r \frac{d\, i_{Lr}}{dt} = V_{in}$$

The solution is:

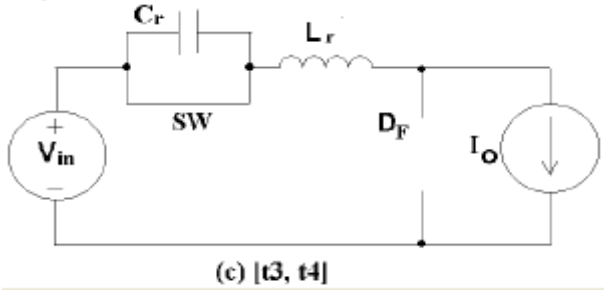
$$i_{Lr} = I_o \cos\alpha + \frac{V_{in}(t - t_2)}{L_r}$$

This state finishes when i_{Lr} reaches the value of output current Io. D_F no longer conducts because its current is now all conducted by Lr.

Duration: $T_{d3} = L_r\, I_o \cos\alpha / V_{in}$

Boundary condition: $i_{Lr}=I_o$

D) Free-wheeling stage [t3, t4]:



Output current freewheels through Lr and switch SW. This stage finishes when the transistor turns off again at t4. t4 is the same as t0 in next cycle.

Duration: Td4= Ts-Td1-Td2-Td3 where Ts is the period of the switching cycle.

5 ACTIVE CLAMP FORWARD CONVERTER

Active clamp is an innovative technique to properly clamp and reset the dc-dc converter's main transformer while achieving low loss, zero voltage transitions of the power switch under wide duty cycle variations without the excessive voltage stress otherwise seen [1].

The detail working principle of active clamp in forward converter is explained as follows [3]. Fig. 7 shows the forward converter with main switch, Q1 and the clamp capacitor Cc with the auxiliary switch, Q2. The transformer model is represented by its Ideal transformer in parallel with a "Magnetizing Inductance" (Lm). Hypothesis before the main switch is conducted; the clamp capacitor's voltage is Vcc.

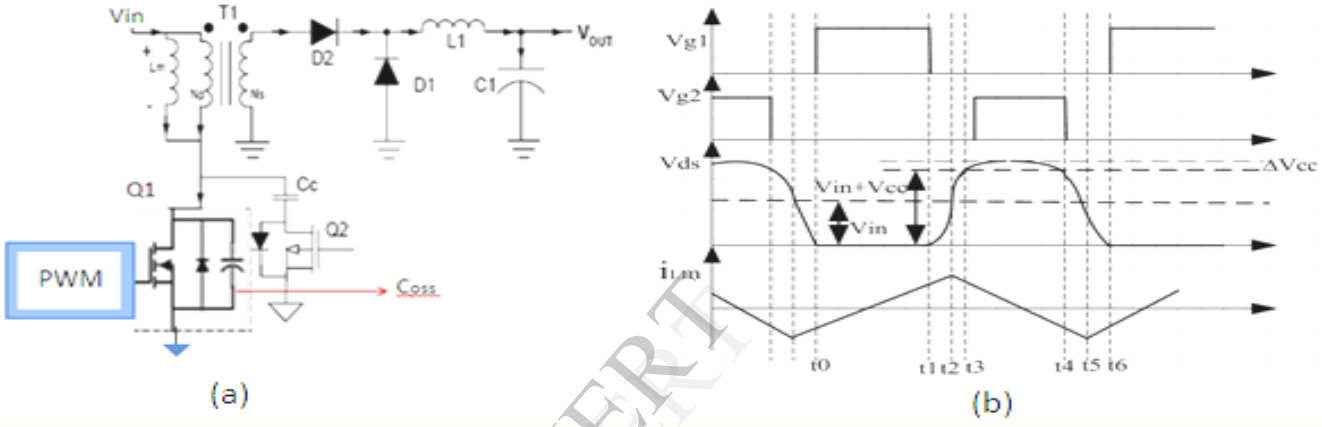


Fig. 7 (a) Active Clamp Forward Circuit and (b) waveform of the main mosfet (Q1) Vds, gate pulses of Q1 and Q2 and magnetizing current, i_{Lm}.

Active clamp switching fundamentals is explained in six distinct switching intervals as follows:

A. t0-t1: Power Transfer Stage

During this state power is transferred to the secondary as the Main Switch, Q1 is conducting and transformer is positive excitation. Magnetizing current changes from the third quadrants of the - I_{Lm} to the first quadrant of the I_{Lm}. The transformer voltage of the primary winding equal to the input voltage Vin;At the same time the secondary rectifier diode conduction, freewheeling diode turn-off, energy from the input power supply through the transformer to the load. While Q1 is conducting the voltage stress Vds is 0, Q2 drain to source voltage is Vin+Vcc.

B. t1-t2: Resonant Stage

In t1 moment, Q1 turned off under ZVS (zero voltage switching). While Q2 is still off, during this stage, Q1 parasitic capacitance Cs and transformer magnetizing inductance Lm resonant .So that the current that reflected from the load current Io/N charge for the Main Switch's junction capacitance Cs ,making

the Q1's Vds rise. In the t2 moment the voltage comes to Vin; while the excitation current of transformer reaches the maximum value I_{Lm}.

C. t2-t3: Resonant Stage

When Magnetizing current of transformer reaches the maximum value, magnetizing inductance Lm and junction capacitance of the Main Switch Cs continued resonance, Q1 drain to source voltage of Vds continues to rise. In t3 moment it reached Vin+Vcc, then the excitation current started to decline namely magnetic core begin to reset.

D. t3-t4: Active Clamp State

At the moment, the body diode of the clamp switch Q2 is conducting, that make the voltage of main switch clamp in Vin+Vcc. Due to the clamp capacitor voltage is now applied across the transformer primary winding, the magnetizing current decreases. In t4 moment reached to a negative maximum value.

E. t4-t5: Resonant Stage

The parasitic capacitance C_{oss} of Q1 again resonant with the excitation inductance Lm and Vds decreased, in the t5 moment, reached to Vin.

F. t5-t6: Resonant Stage

Vds continues to decline, in t6, it dropped to 0. At the completion of t6, the switching cycle reverts back to the t0-t1 state and the sequence repeats.

Apart from resetting the transformer, in active clamp there are significant benefits such as recycling transformer magnetizing energy instead of dissipating it in a resistor in case of RCD reset, facilitates zero voltage transition of the main switch for higher efficiency.

6 PRACTICAL ACTIVE CLAMP FORWARD CONVERTER

A 50W active clamp forward converter with input range 16-50V; 400 KHz operating frequency is implemented using PWM controller UCC2891 [4]; in order to verify whether the ZVS phenomenon is happening in active clamp converter. Theoretically the main switch could achieve ZVS by the resonant circuit; which includes the junction capacitance *Coss*, the leakage inductance and the magnetizing inductance Lm. The main mosfet switching waveform is analyzed under zero voltage condition as follow.

Fig. 8 shows the Vds of the main mosfet at input voltage 16V. It can be seen that the Vds is being clamped at voltage 40V during the turn off period; which is greater than twice of Vin; (i.e. > 2*16=32V); which is the basic condition in active clamp reset.

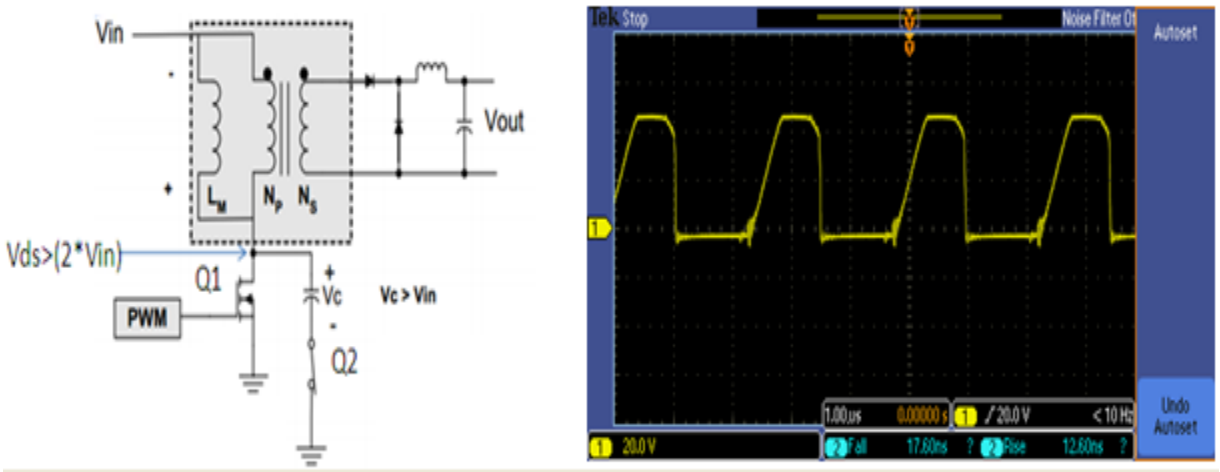


Fig. 8 (a) Active clamp forward converter equivalent circuit during main switch turn off and (b) corresponding drain waveform at input voltage 16V.

As it can be observe from fig. 8 that the polarity across the transformer primary winding is reversed during the turn off of the main switch. The reversed voltage will force the magnetizing current to reverse slope and reset the magnetizing current.

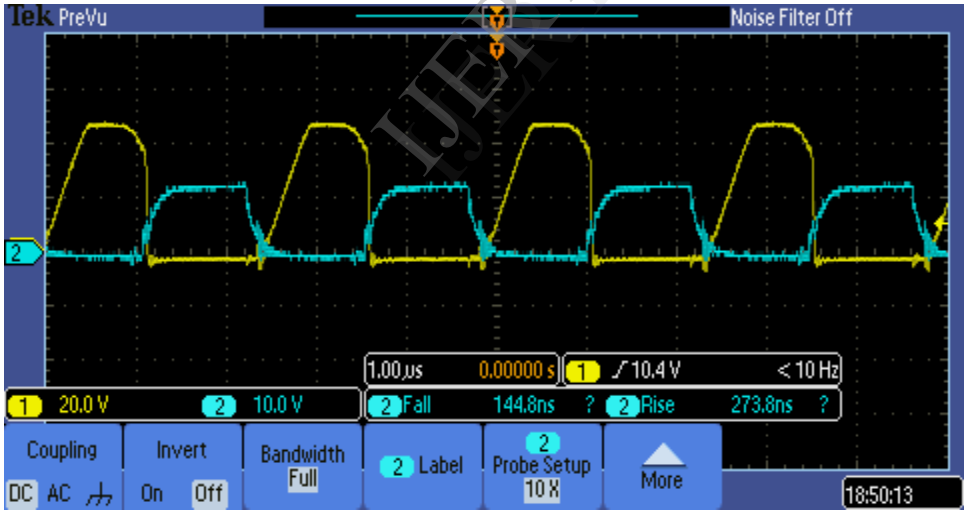


Fig. 9 Gate and drain waveform at input voltage 16V.

From the fig. 9 above further analyses is made during the turn off and turn on of the main switch as follows:

A) Main Switch Zero Voltage Turn-off Transition:

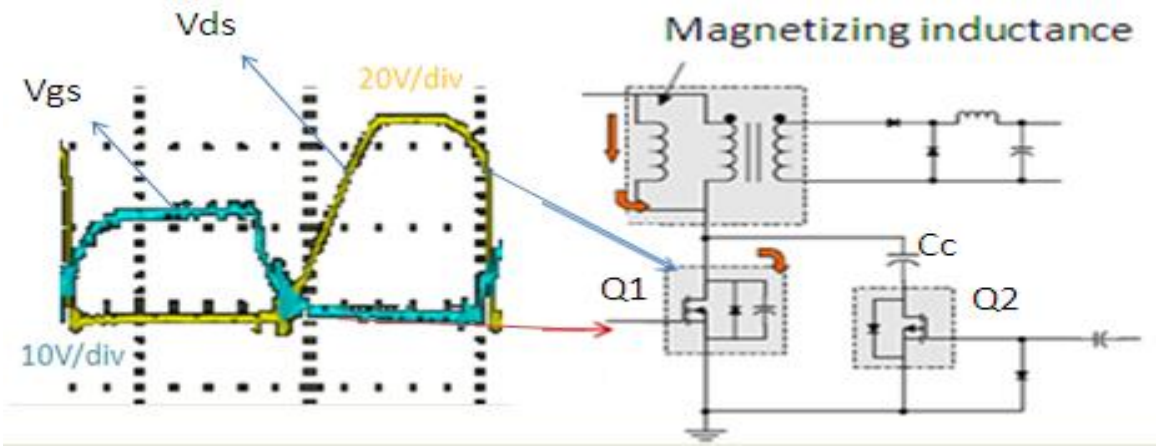


Fig. 10 ZVS of the main mosfet during turn off.

When the main switch is on, and all the current is flowing through the main switch. When the gate voltage drops, if the gate voltage is visualize as analogous to the channel current, if the gate can be turn off very, very quickly then basically the flow of current through the main MOSFET is stop before the voltage gets a chance to rise. The reason why the voltage doesn't rise quickly is because of the capacitance associated with the FET itself. So it can be seen from the fig. 10 that a zero volt switching event occurs during turn off of the main switch, Q1.

B) Main Switch Zero Voltage Turn-on Transition:

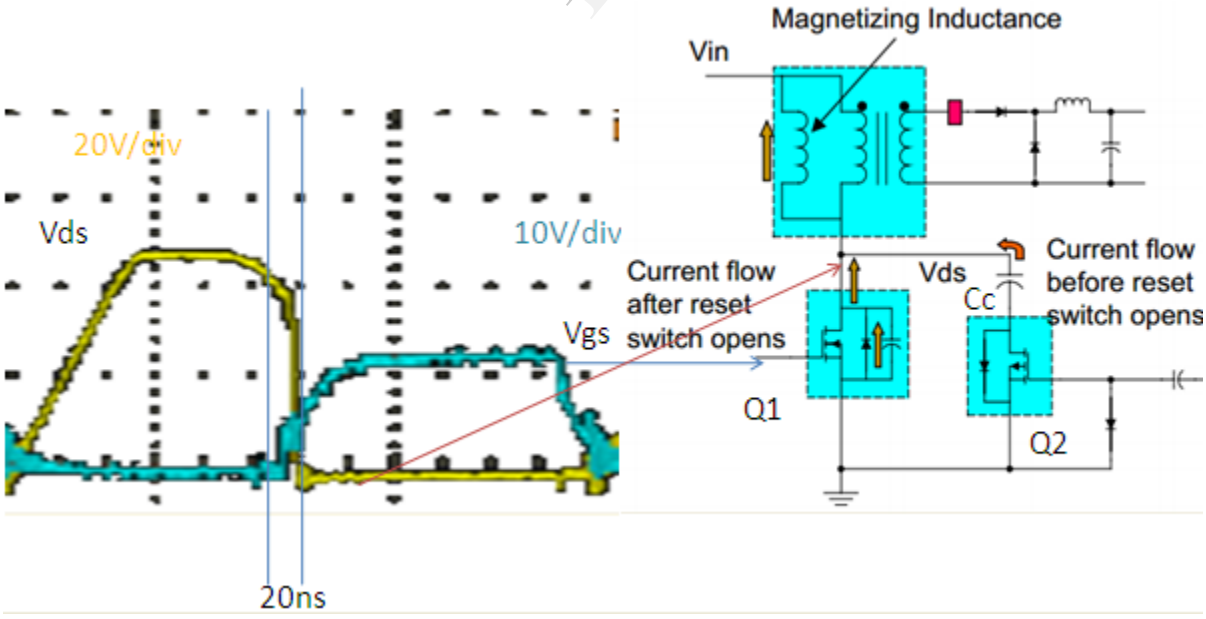


Fig. 11 ZVS of the main mosfet during turn on.

Theoretically it is possible to get zero voltage switching for the main FET turn on. The idea here is that when the active clamp switch is turned on, a current is flowing up through the capacitor, through the magnetizing inductance and up and back to the Vin source. If the switch is off, it immediately stop the flow of current through the capacitor. The current flowing up through the magnetizing inductance wants to continue to flow and it will tend to pull the voltage down on the drain and so potentially a zero volt switching is achieved here. In a practical application it's hard to do, since the secondary side starts to affect the zero volt switching. As seen in the fig. 11 that the main switch is not switched at zero voltage; as indicated by the overlap between Vds and Vgs of about 20ns**.** An additional circuit is required to actually implement ZVS during turn on.

7 CONCLUSIONS

Soft switching and active clamp techniques are discussed in detailed. ZVS in active clamp forward converter is investigated. However, in the practical implementation of the active clamp forward converter; it is found that ZVS during turn off is achieved while during the turn on of the main switch; there is overlap of about 20ns between Vds and Vgs. But compare to all other techniques of transformer reset; active clamp have been proves to be more advantageous. Although somebody have propose method to achieve ZVS during turn on of main switch by implementing auxiliary network for the auxiliary switch Q2 [7]; the new technology is not perfect. So we have to consider how to make its advantages be reflected greatly in low-to-medium power applications.

References:

1) Bill Andreycak; "Active clamp and reset technique enhances forward converter performance", Oct. 1994; Texas Insrument.

2) Per Karlsson, Martin Bojrup, Mats Alaküla and Lars Gertmar; " Zero Voltage Switching Converters".

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